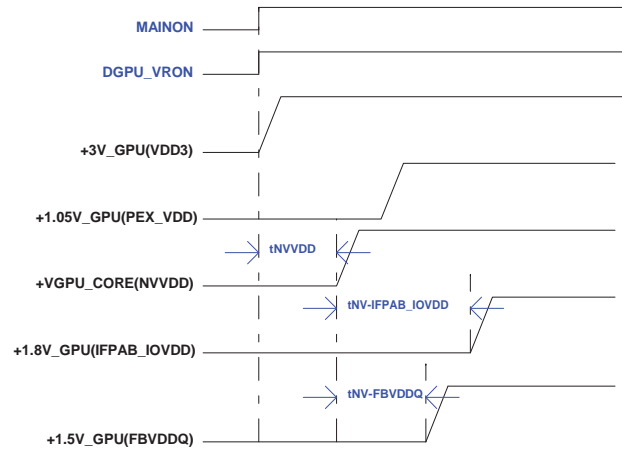




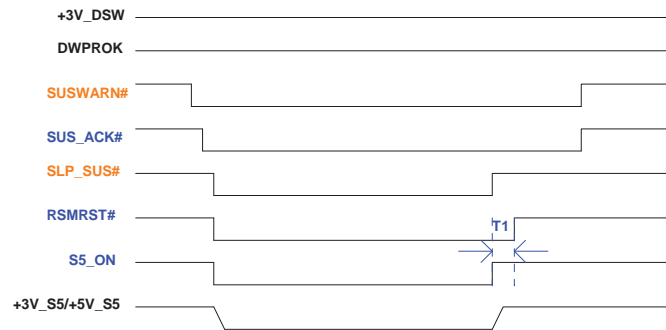
N12P-GE Power Up Sequence



N12P-GE Power up Sequence

tINVDD>0
tINV-IFPAB_IOVDD>0
tINV-FBVDDQ>0

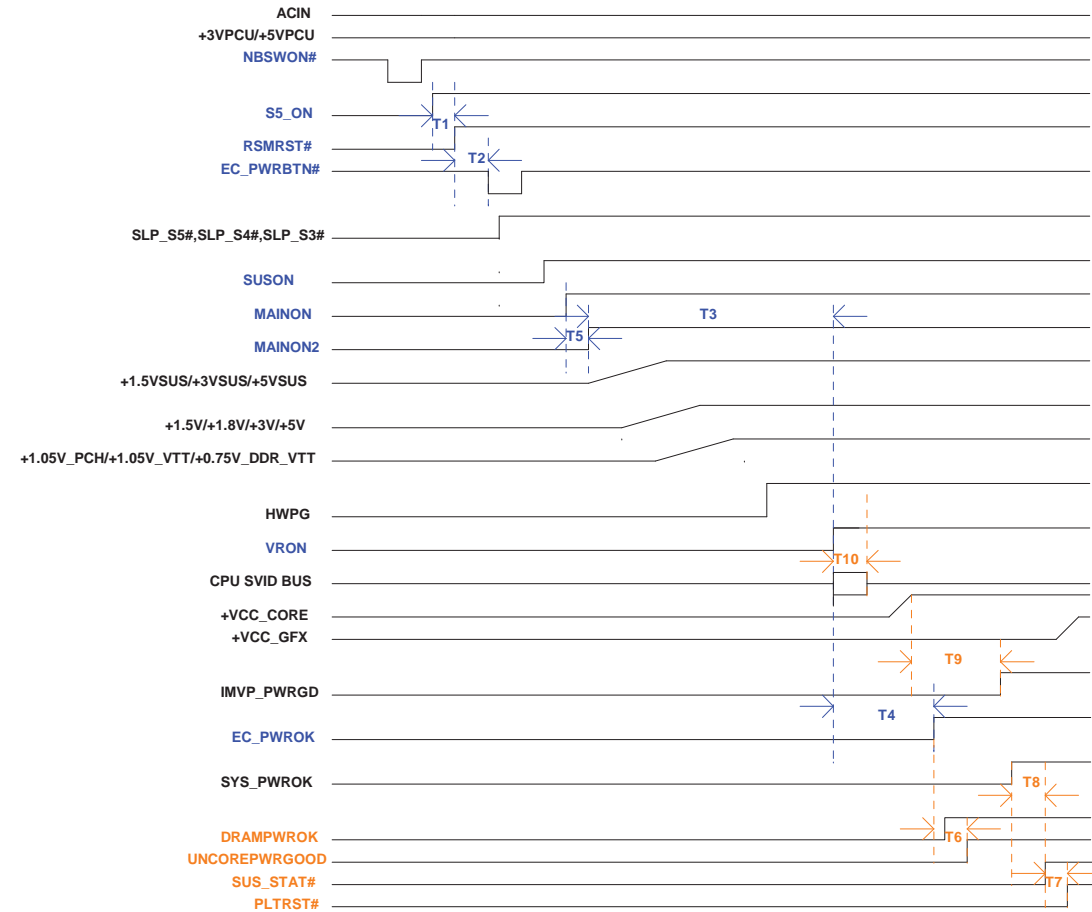
Deep S4/S5 off-on Sequence



Deep S4/S5 Sequence

T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence

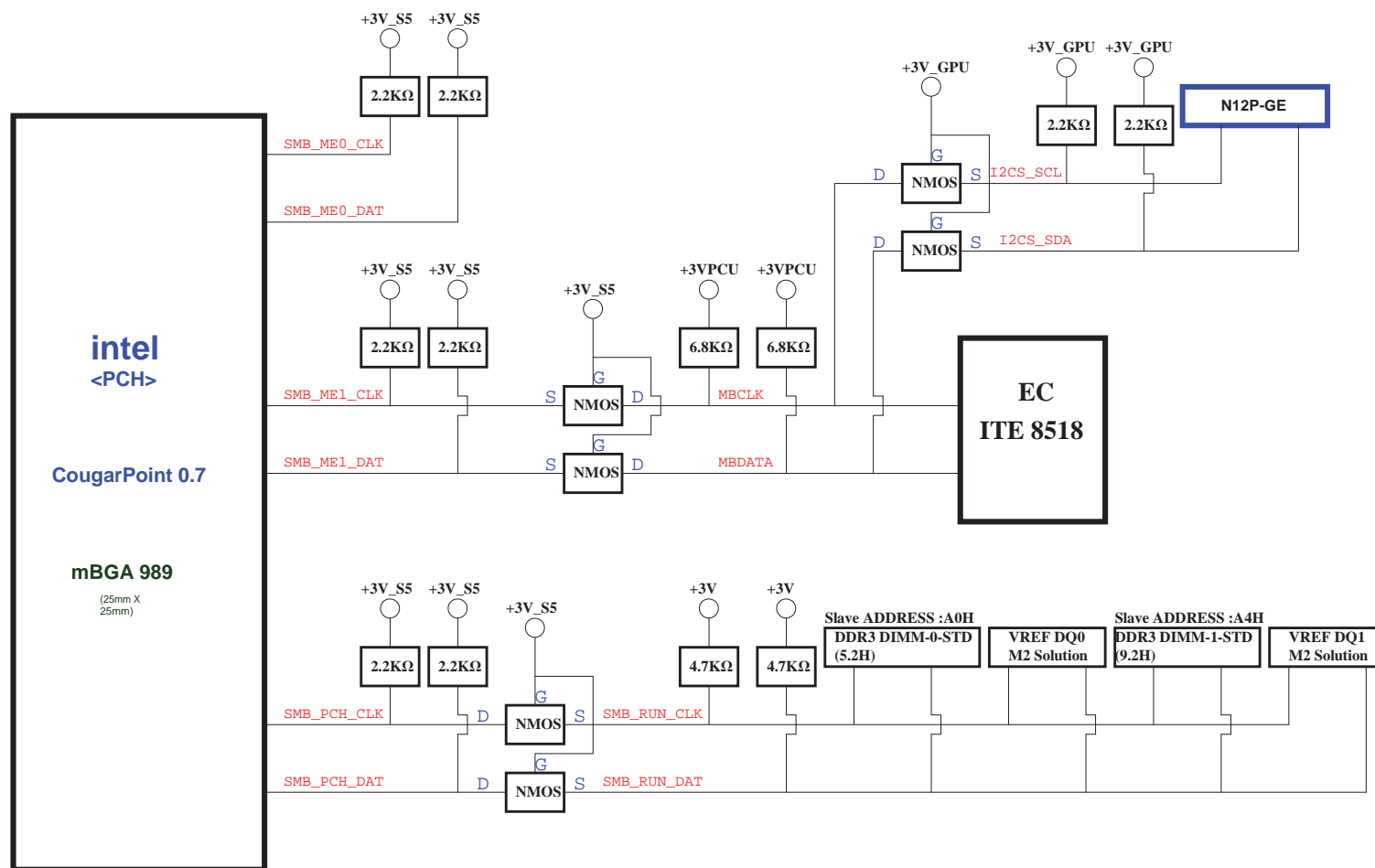


System Power Sequence

T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
T5: MAINON TO MAINON2 = 500us
T6: EC_PWROK to UNCOREPWROGOOD = 2ms(Min)
T7: SUS_STAT# to PLTRST# = 60us(Min)
T8: SYS_PWROK to SUS_STAT# = 1ms(Min)
T9: +VCC_CORE to IMVP_PWRGD = 5ms(Max)
T10: VRON to accept SVID command. = 5ms(Max)



Quanta Computer Inc.
PROJECT : ZRJ

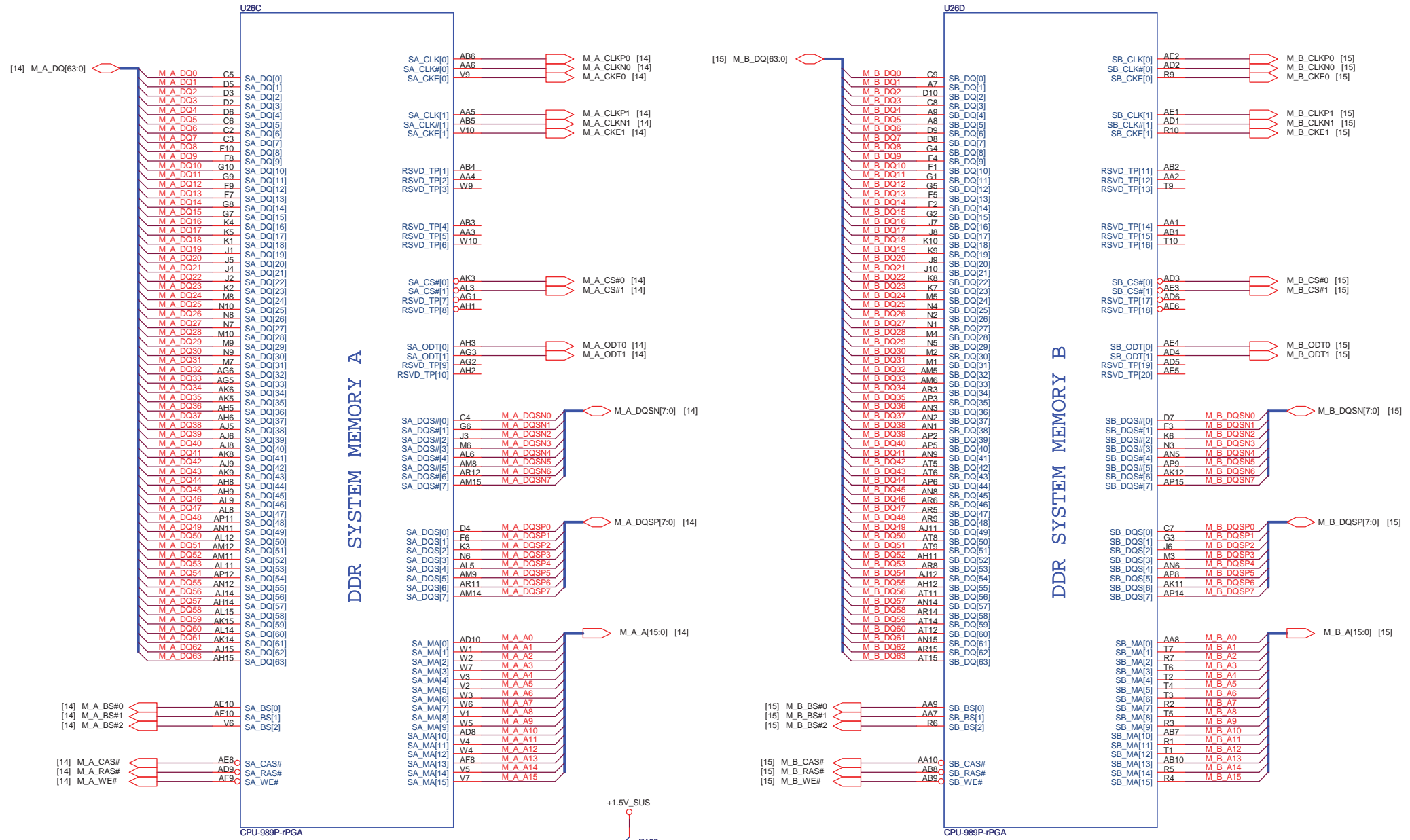


Sandy Bridge Processor (CLK,MISC,JTAG)

[illegible]

Sandy Bridge Processor (DDR3)

05



Quanta Computer Inc.

PROJECT : ZRJ

POWER

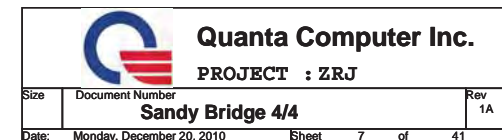
Real
10uF x 6



Sandy Bridge Processor (RESERVED, CFG)

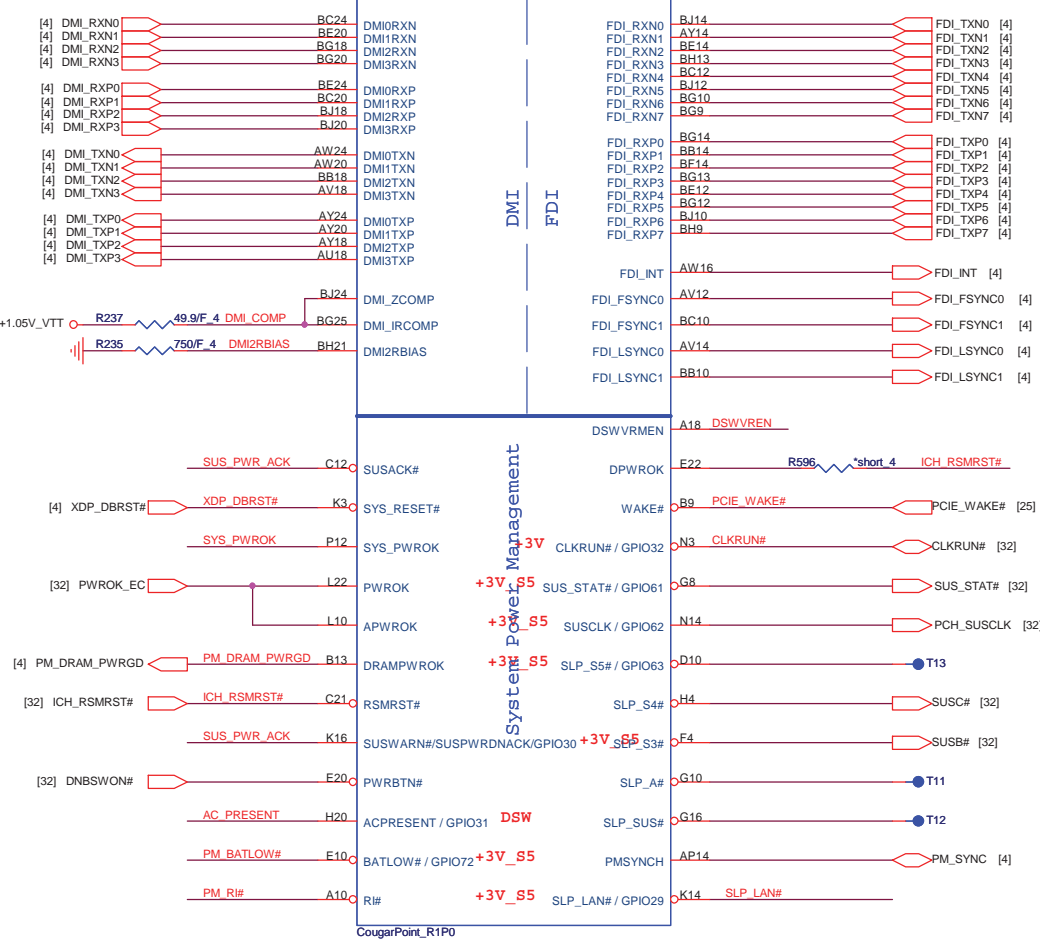
The diagram illustrates the pinout for the CPU-989P-rPGA package. It shows two rows of pins, with the left row numbered 1 to 100 and the right row numbered 101 to 200. Each pin is labeled with a name, typically starting with 'VSS' followed by a number (e.g., VSS1, VSS2, VSS3, etc.). The central label 'VSS' indicates that these pins are ground connections. The package is labeled 'CPU-989P-rPGA' at the bottom.

Pin Number	Pin Name	Pin Number	Pin Name
1	VSS1	101	VSS101
2	VSS2	102	VSS102
3	VSS3	103	VSS103
4	VSS4	104	VSS104
5	VSS5	105	VSS105
6	VSS6	106	VSS106
7	VSS7	107	VSS107
8	VSS8	108	VSS108
9	VSS9	109	VSS109
10	VSS10	110	VSS110
11	VSS11	111	VSS111
12	VSS12	112	VSS112
13	VSS13	113	VSS113
14	VSS14	114	VSS114
15	VSS15	115	VSS115
16	VSS16	116	VSS116
17	VSS17	117	VSS117
18	VSS18	118	VSS118
19	VSS19	119	VSS119
20	VSS20	120	VSS120
21	VSS21	121	VSS121
22	VSS22	122	VSS122
23	VSS23	123	VSS123
24	VSS24	124	VSS124
25	VSS25	125	VSS125
26	VSS26	126	VSS126
27	VSS27	127	VSS127
28	VSS28	128	VSS128
29	VSS29	129	VSS129
30	VSS30	130	VSS130
31	VSS31	131	VSS131
32	VSS32	132	VSS132
33	VSS33	133	VSS133
34	VSS34	134	VSS134
35	VSS35	135	VSS135
36	VSS36	136	VSS136
37	VSS37	137	VSS137
38	VSS38	138	VSS138
39	VSS39	139	VSS139
40	VSS40	140	VSS140
41	VSS41	141	VSS141
42	VSS42	142	VSS142
43	VSS43	143	VSS143
44	VSS44	144	VSS144
45	VSS45	145	VSS145
46	VSS46	146	VSS146
47	VSS47	147	VSS147
48	VSS48	148	VSS148
49	VSS49	149	VSS149
50	VSS50	150	VSS150
51	VSS51	151	VSS151
52	VSS52	152	VSS152
53	VSS53	153	VSS153
54	VSS54	154	VSS154
55	VSS55	155	VSS155
56	VSS56	156	VSS156
57	VSS57	157	VSS157
58	VSS58	158	VSS158
59	VSS59	159	VSS159
60	VSS60	160	VSS160
61	VSS61	161	VSS161
62	VSS62	162	VSS162
63	VSS63	163	VSS163
64	VSS64	164	VSS164
65	VSS65	165	VSS165
66	VSS66	166	VSS166
67	VSS67	167	VSS167
68	VSS68	168	VSS168
69	VSS69	169	VSS169
70	VSS70	170	VSS170
71	VSS71	171	VSS171
72	VSS72	172	VSS172
73	VSS73	173	VSS173
74	VSS74	174	VSS174
75	VSS75	175	VSS175
76	VSS76	176	VSS176
77	VSS77	177	VSS177
78	VSS78	178	VSS178
79	VSS79	179	VSS179
80	VSS80	180	VSS180
81	VSS81	181	VSS181
82	VSS82	182	VSS182
83	VSS83	183	VSS183
84	VSS84	184	VSS184
85	VSS85	185	VSS185
86	VSS86	186	VSS186
87	VSS87	187	VSS187
88	VSS88	188	VSS188
89	VSS89	189	VSS189
90	VSS90	190	VSS190
91	VSS91	191	VSS191
92	VSS92	192	VSS192
93	VSS93	193	VSS193
94	VSS94	194	VSS194
95	VSS95	195	VSS195
96	VSS96	196	VSS196
97	VSS97	197	VSS197
98	VSS98	198	VSS198
99	VSS99	199	VSS199
100	VSS100	200	VSS200



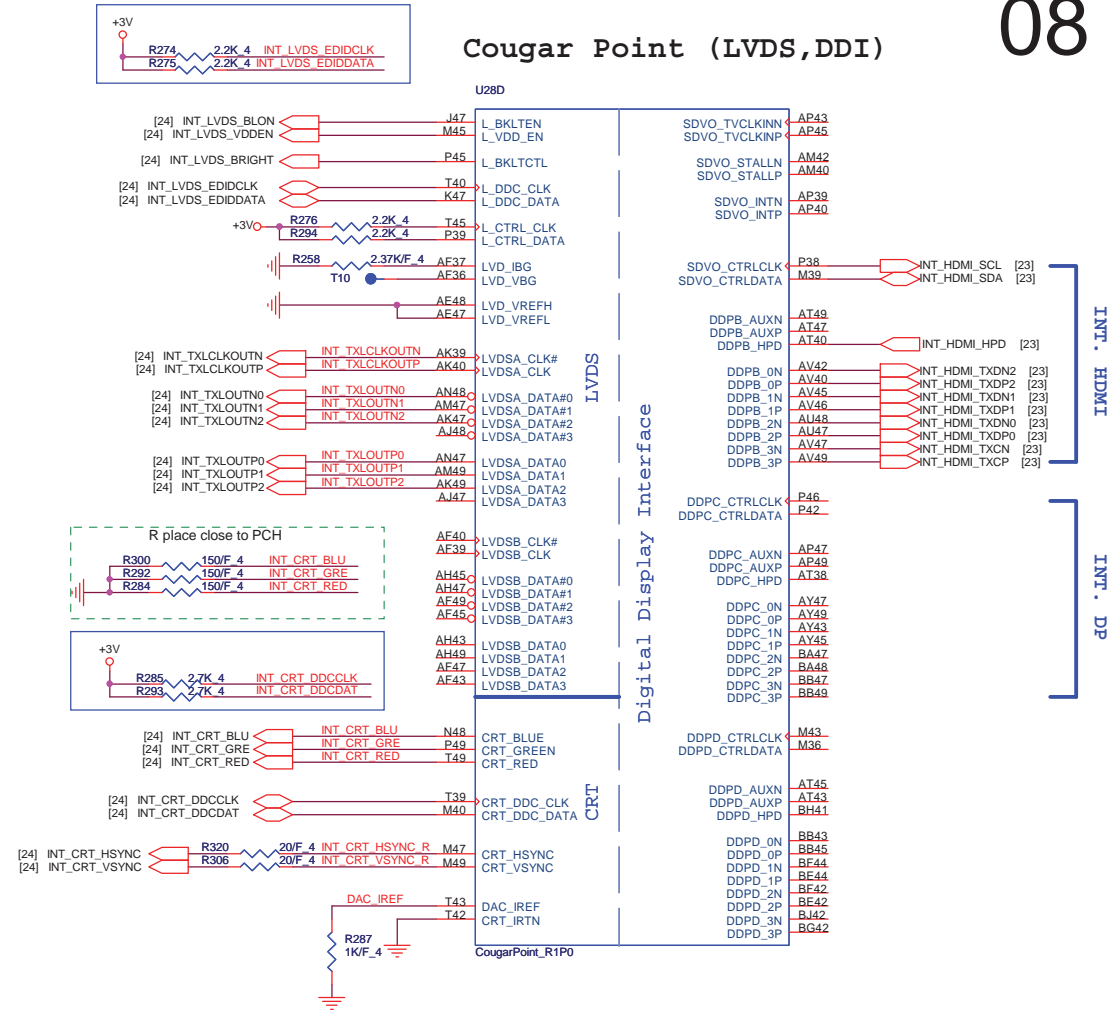
Cougar Point (DMI, FDI, PM)

U28C

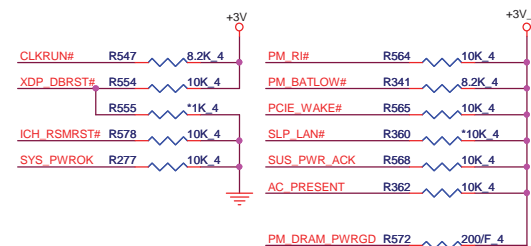


Cougar Point (LVDS, DDI)

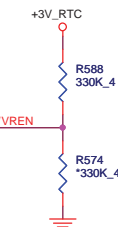
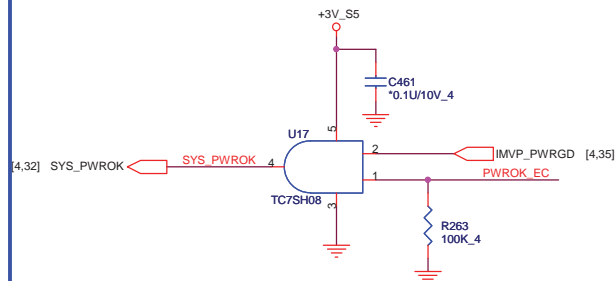
U28D



PCH Pull-high/low(CLG)



System PWR_OK(CLG)

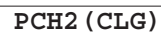


```
On Die DSW VR Enable
```

High = Enable (Default)

Low = Disable

09

[illegible]

[28] ACZ_BITCLK	R343	33_4	ACZ_BITCLK R
[28] ACZ_SYNC	R347	33_4	ACZ_SYNC R
[28] ACZ_RST#	R364	33_4	ACZ_RST# R
[28] ACZ_SDOUT	R597	33_4	ACZ_SDOUT R

PCH_SPI_CS0# 1
 PCH_SPI_CLK 2
 PCH_SPI_CK 3
 PCH_SPI_SI 4
 PCH_SPI_SO 5

R533 ~short 4 PCH_SPI1_CLK_R 1
 R529 ~short 4 PCH_SPI1_SI_R 2
 R536 ~short 4 PCH_SPI1_SO_R 3
 R538 3.3K 4

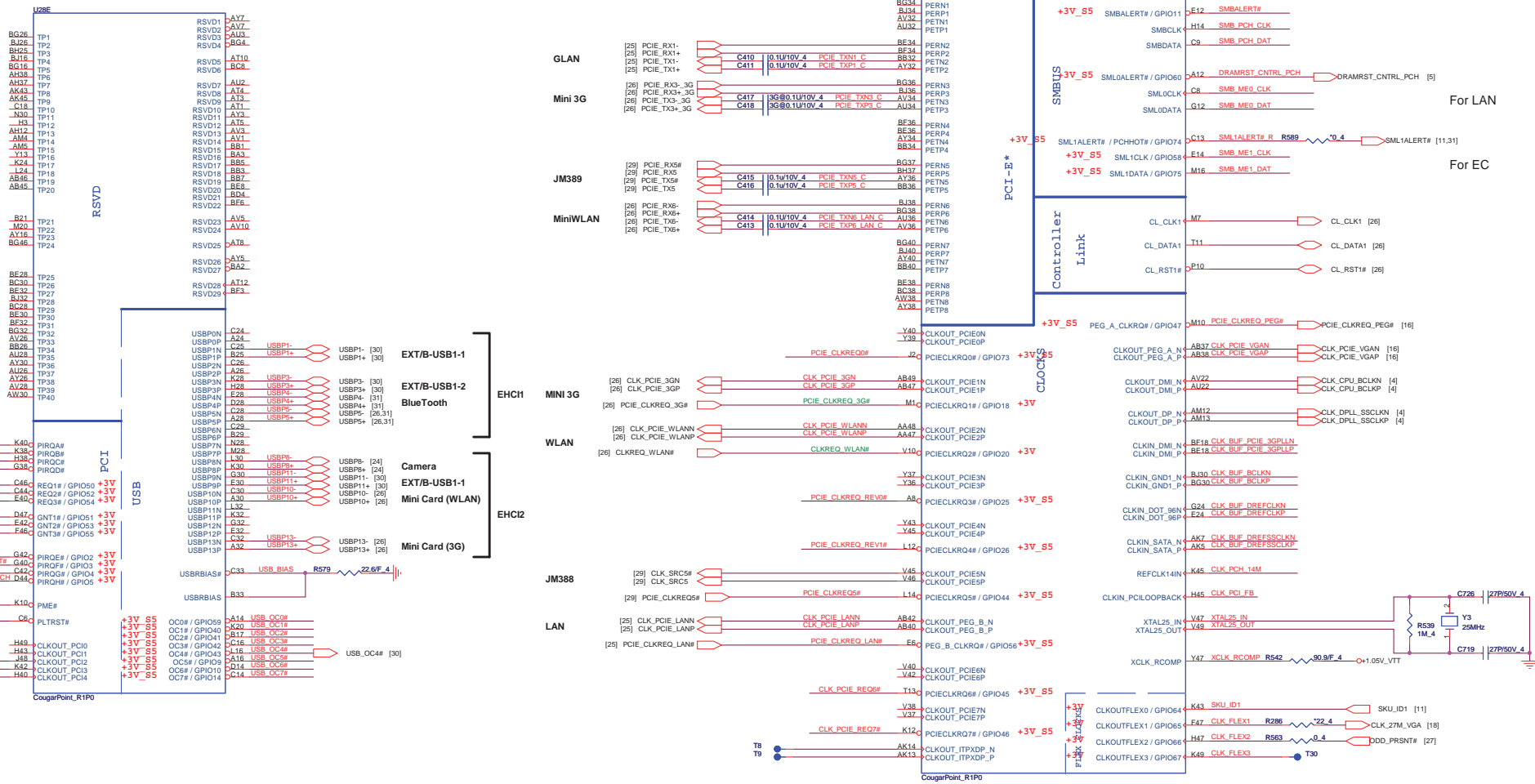
C720 22pF/50V_4
 C724 0.1uF/10V_4

REV: B modify footprint

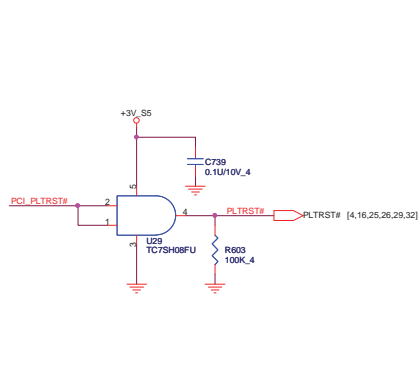
Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI *</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	<p>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</p>
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)										
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

Cougar Point-M (PCI,USB,NVRAM)

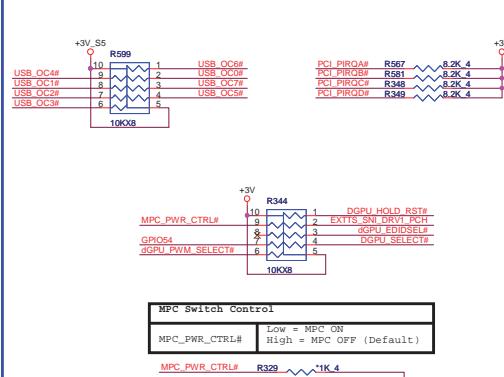
Cougar Point-M (PCI-E,SMBUS,CLK)



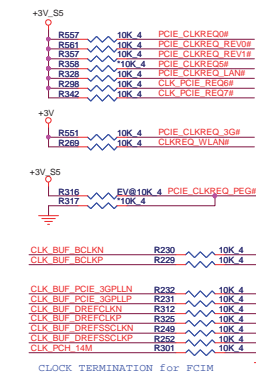
PLTRST#(CLG)



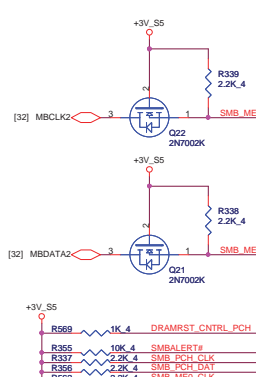
PCI/USB0C# Pull-up(CLG)



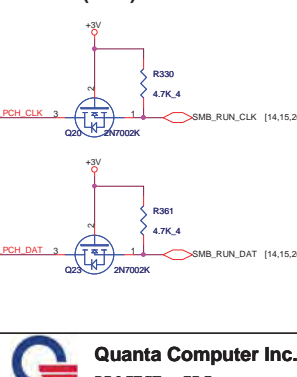
CLK_REQ/Strap Pin(CLG)

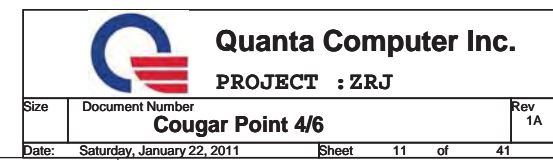
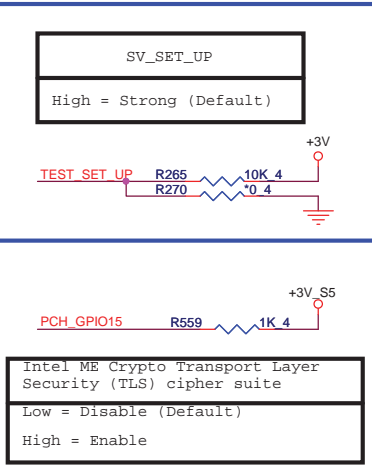
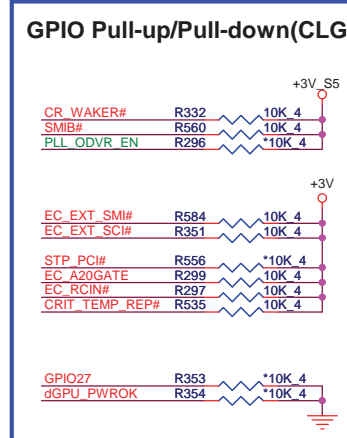
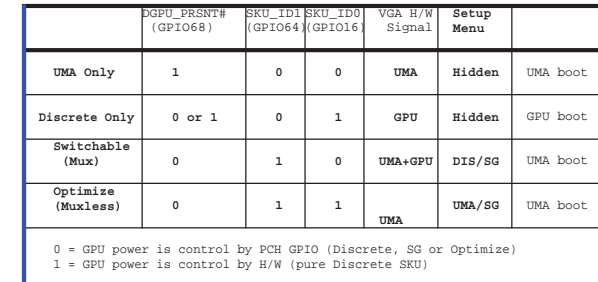


SMBus/Pull-up(CLG)

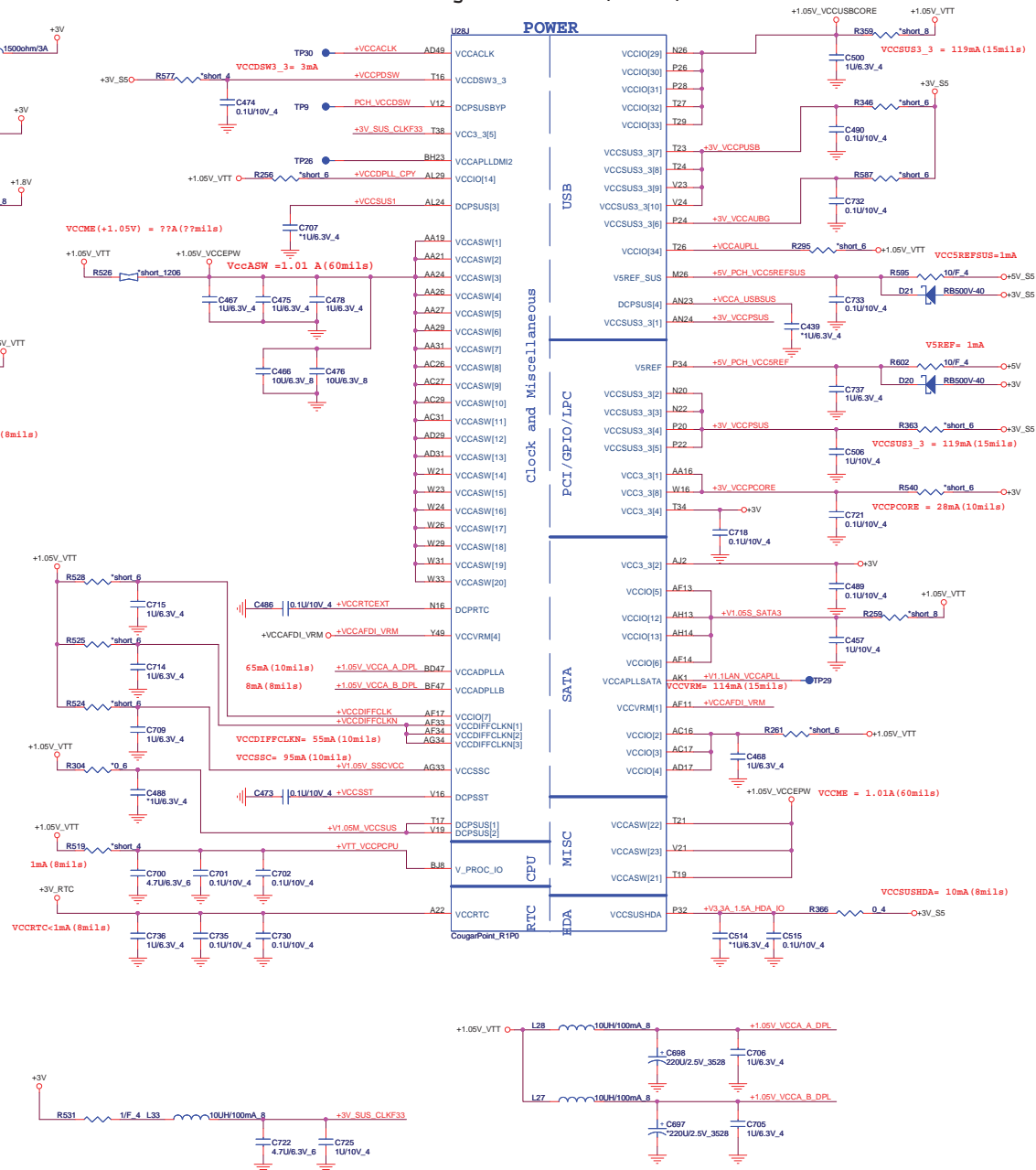


SMBus(PCH)

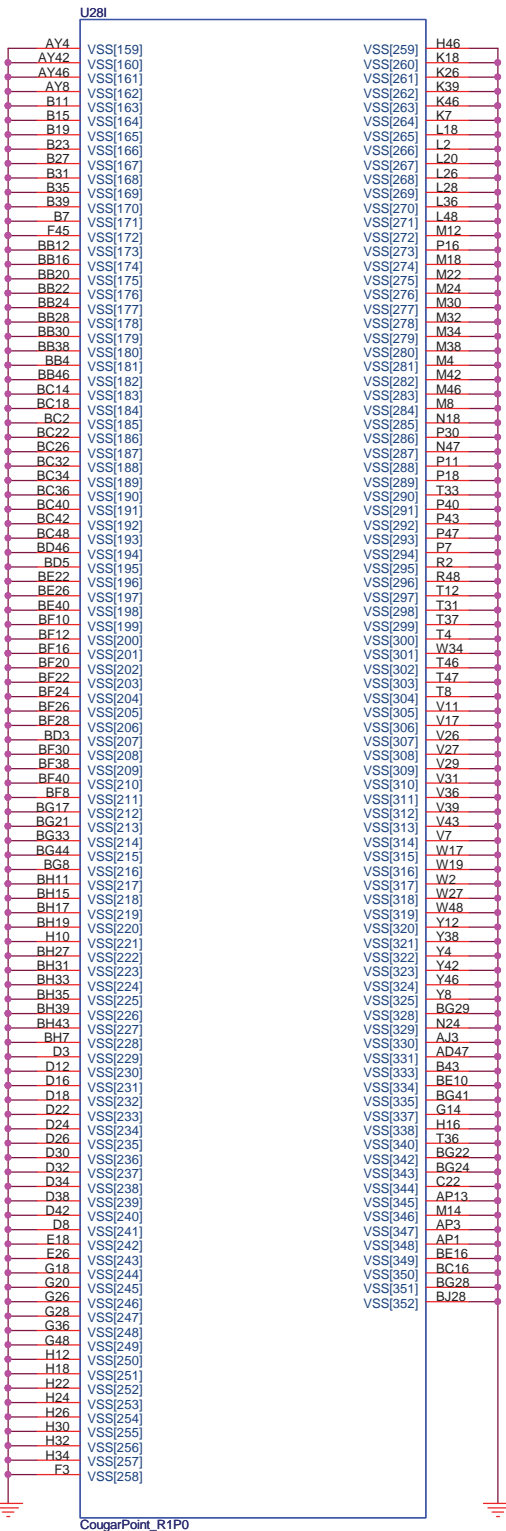
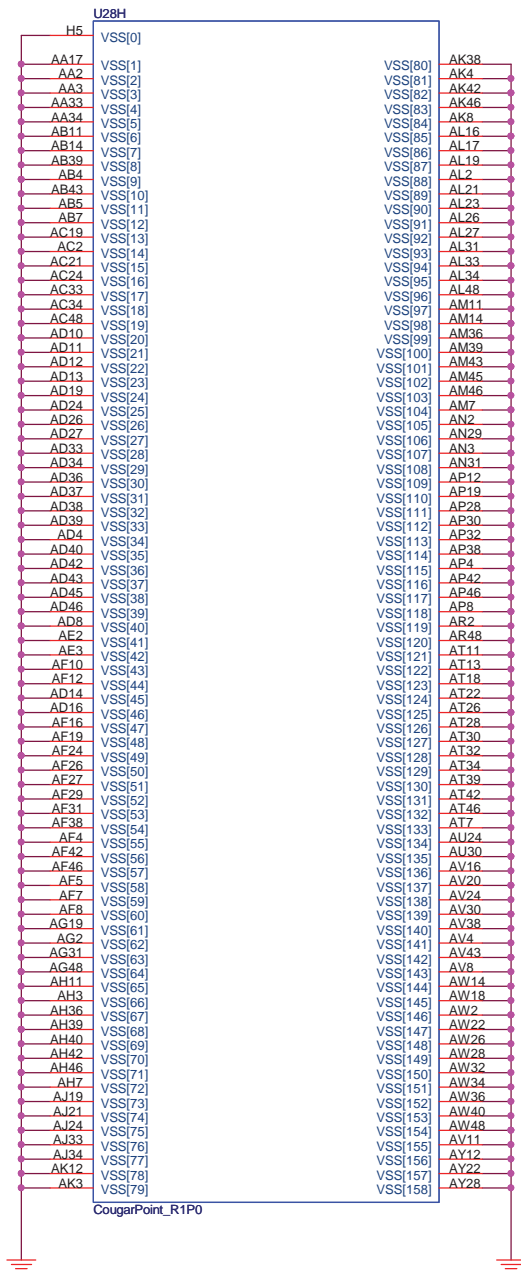




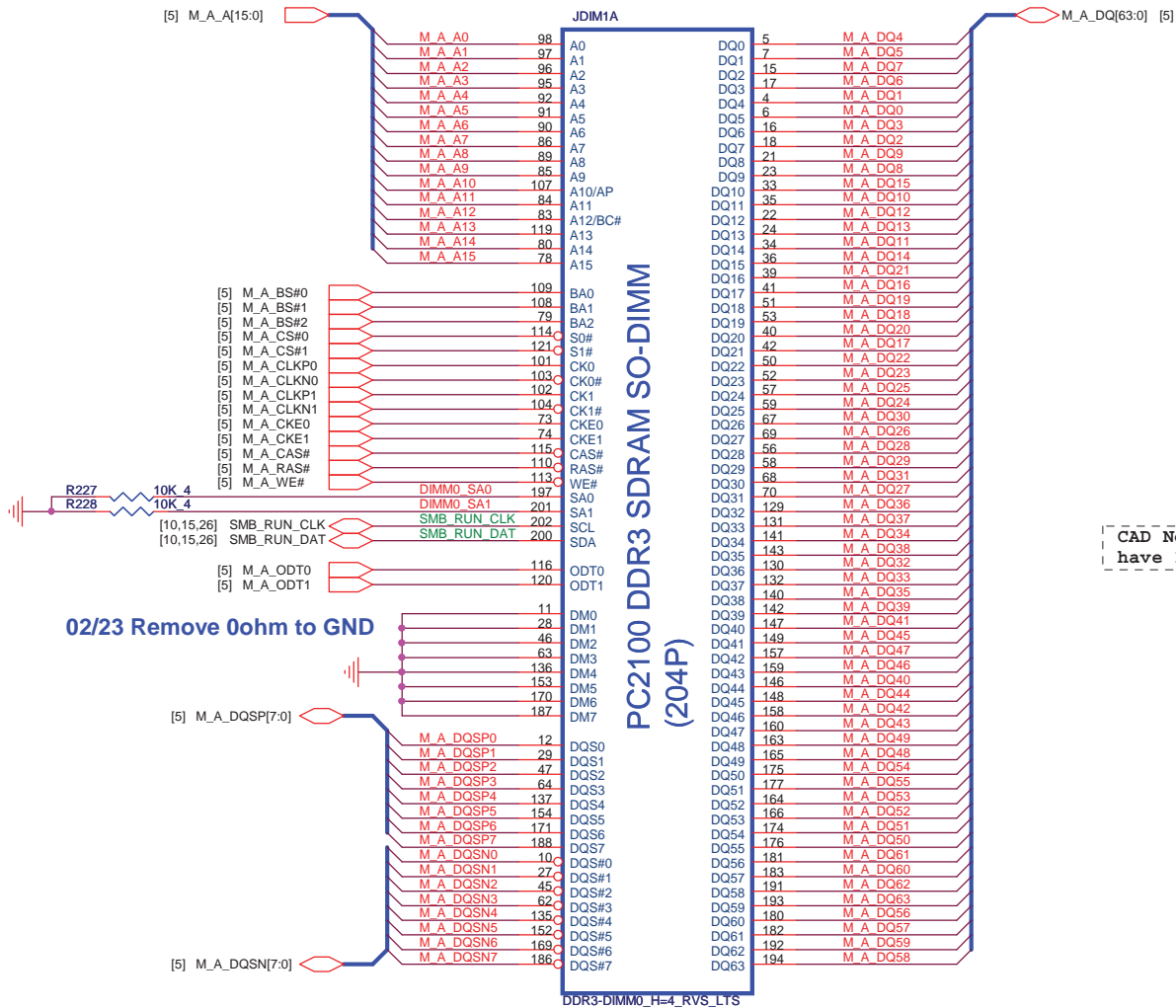
Cougar Point-M (POWER)



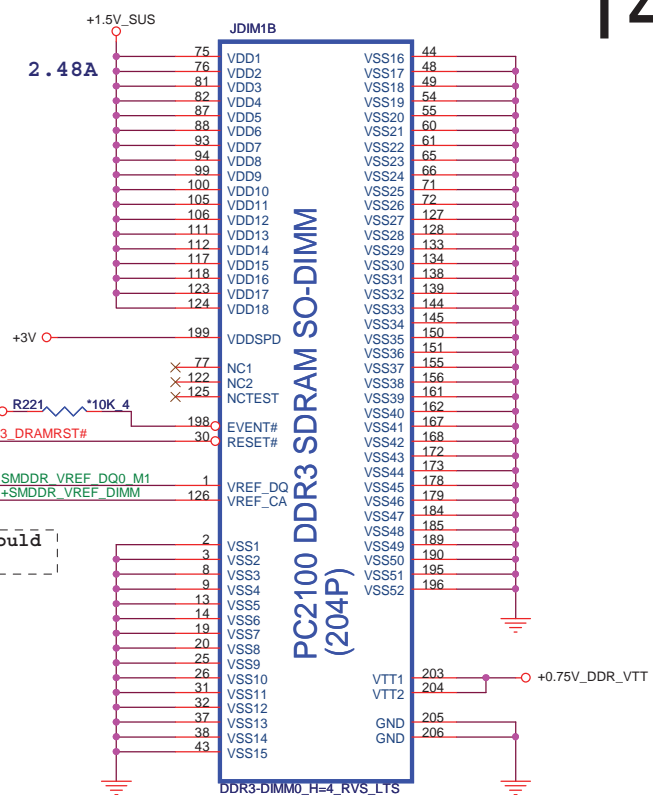
IBEX PEAK-M (GND)



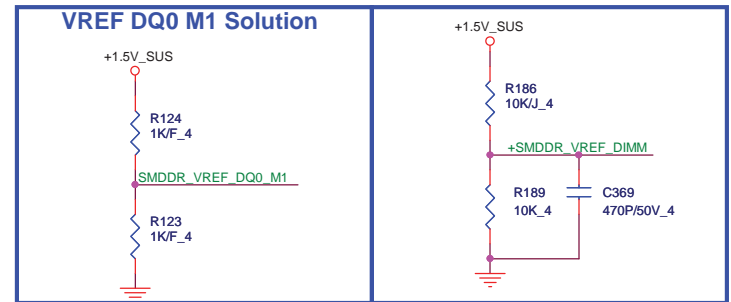
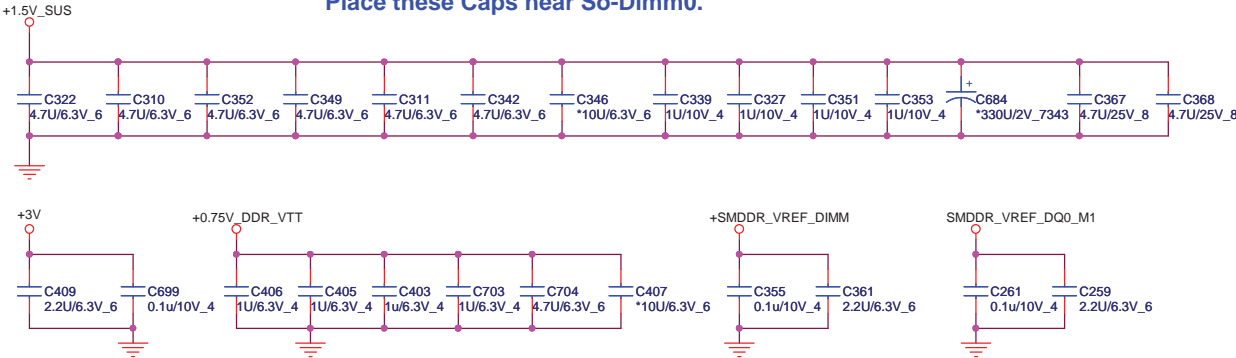
DDR STD (DDR)



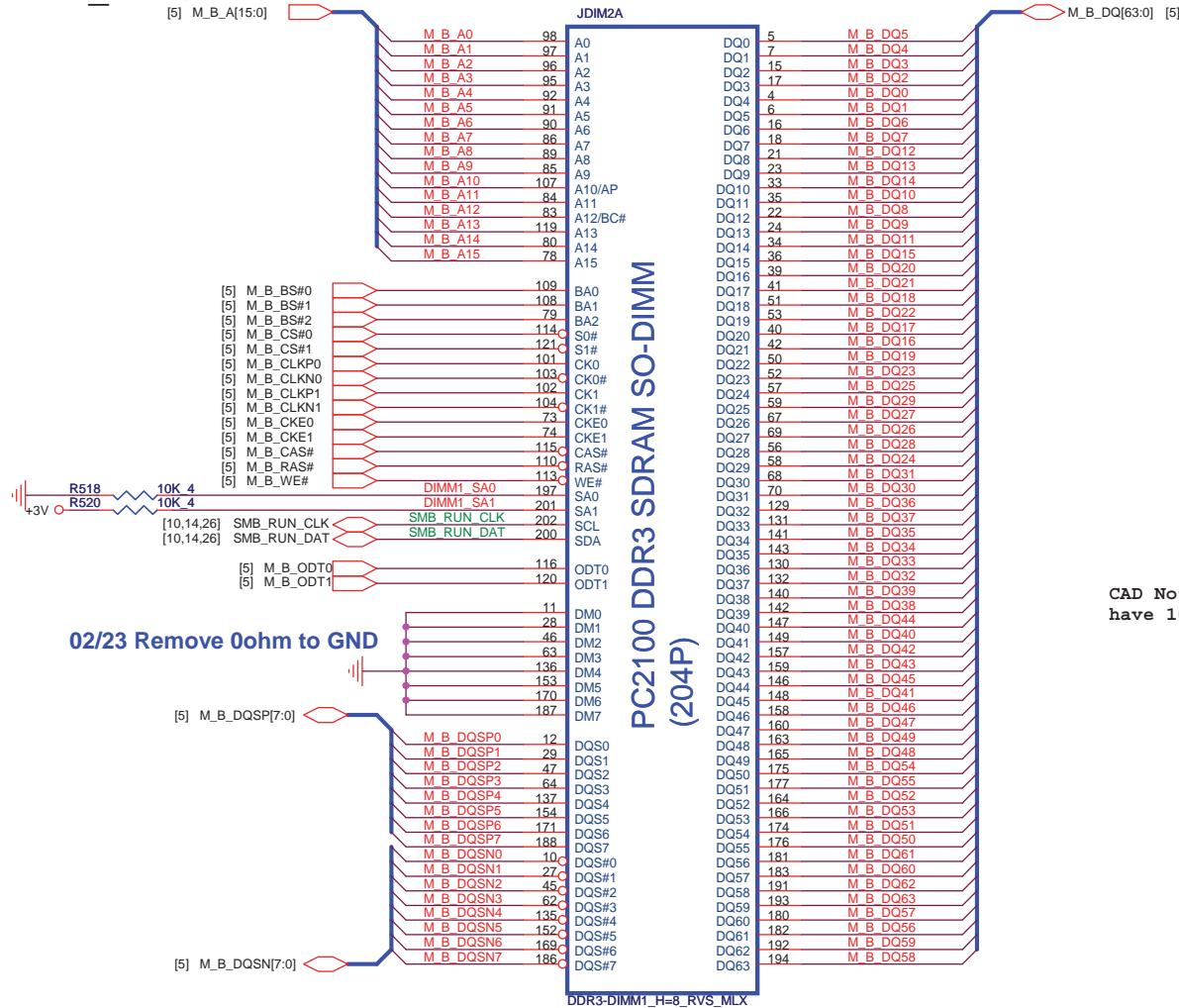
CAD Note: All VREF traces should have 10 mil trace width



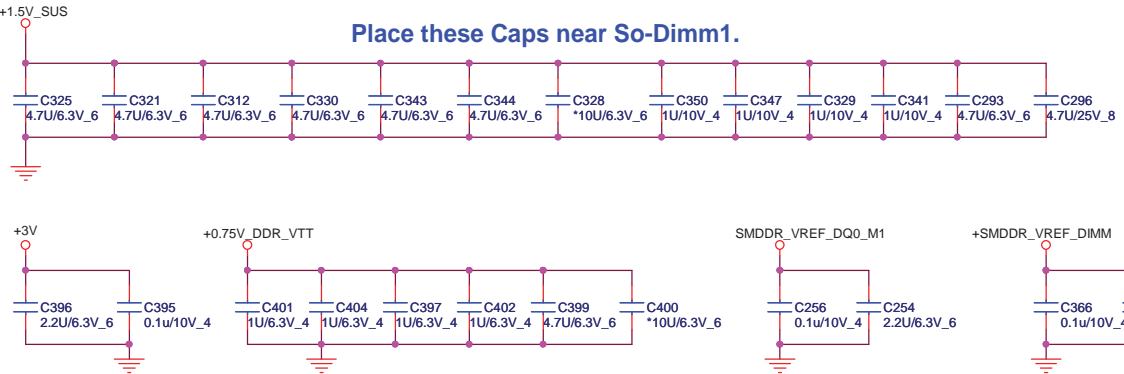
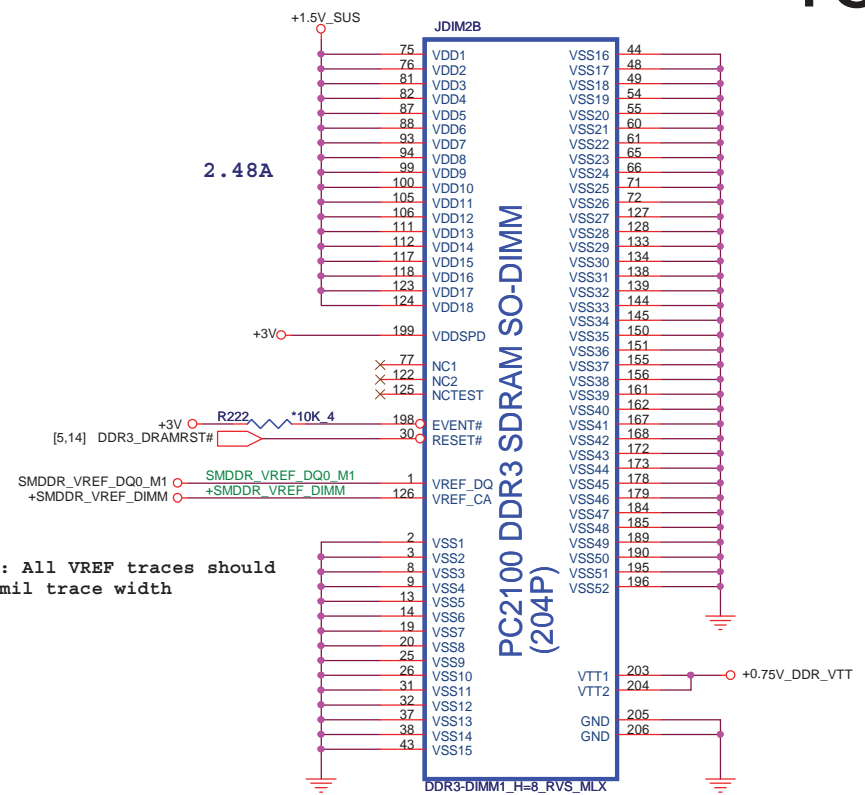
Place these Caps near So-Dimm0.




DDR_RVS (DDR)



CAD Note: All VREF traces should have 10 mil trace width



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

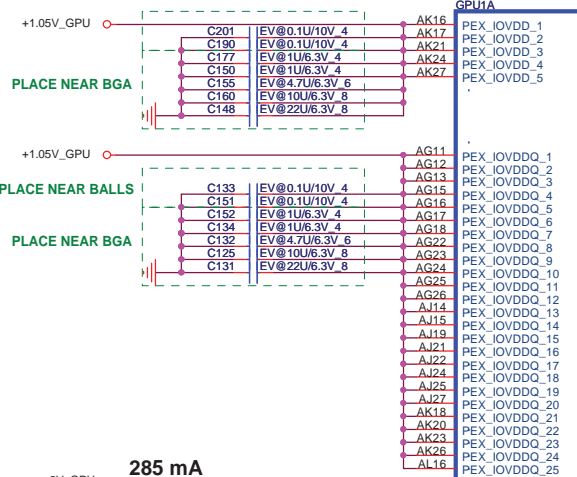


Quanta Computer Inc.
PROJECT : ZRJ

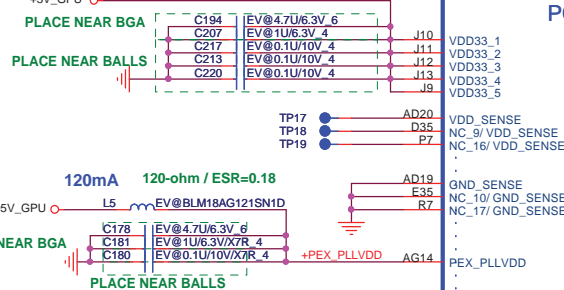
Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date:	Saturday, January 22, 2011	Sheet 15 of 41

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

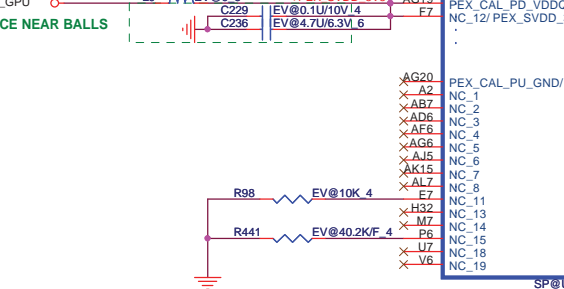
2200mA
PLACE NEAR BALLS



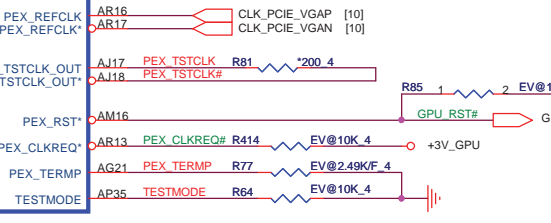
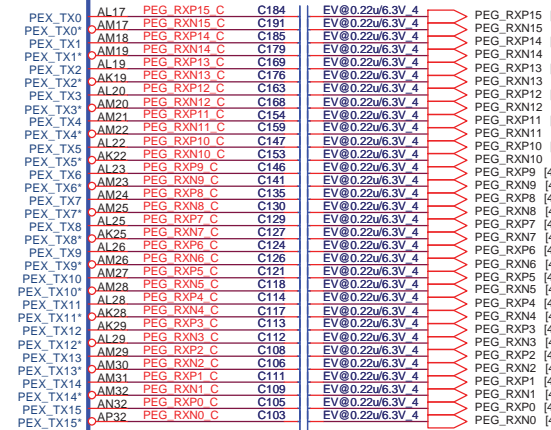
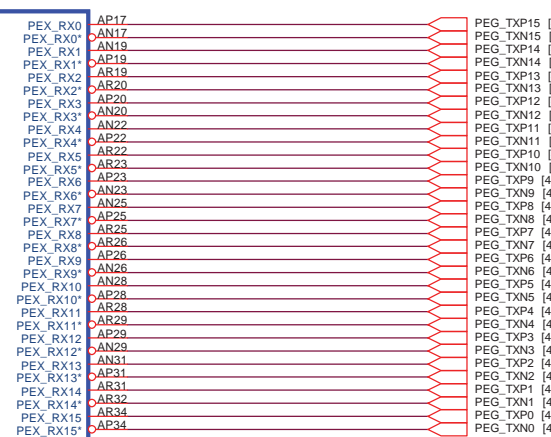
+3V_GPU 285 mA



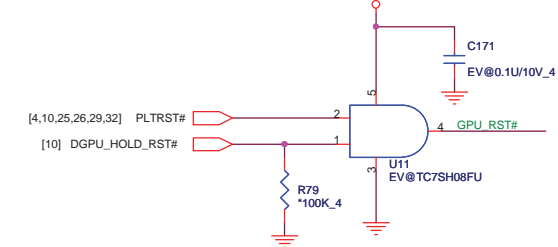
+3V_GPU 120mA



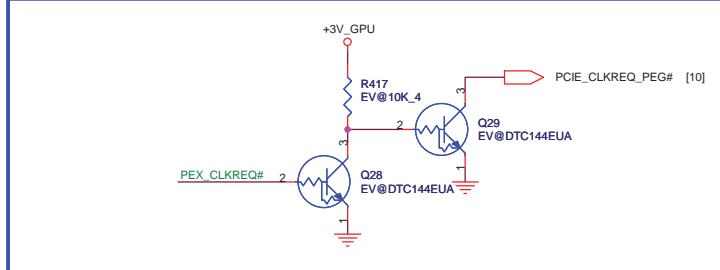
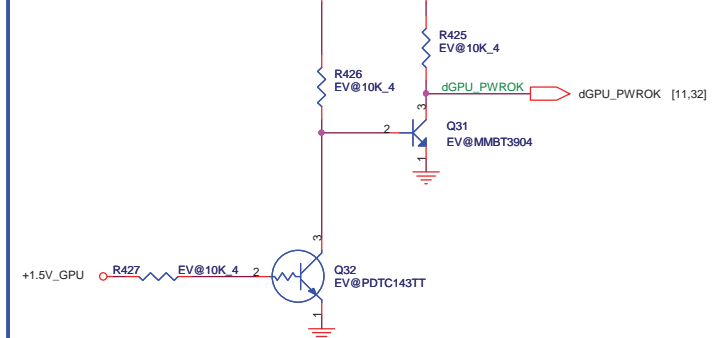
PCI EXPRESS



GPU RST#



GPU all PWROK

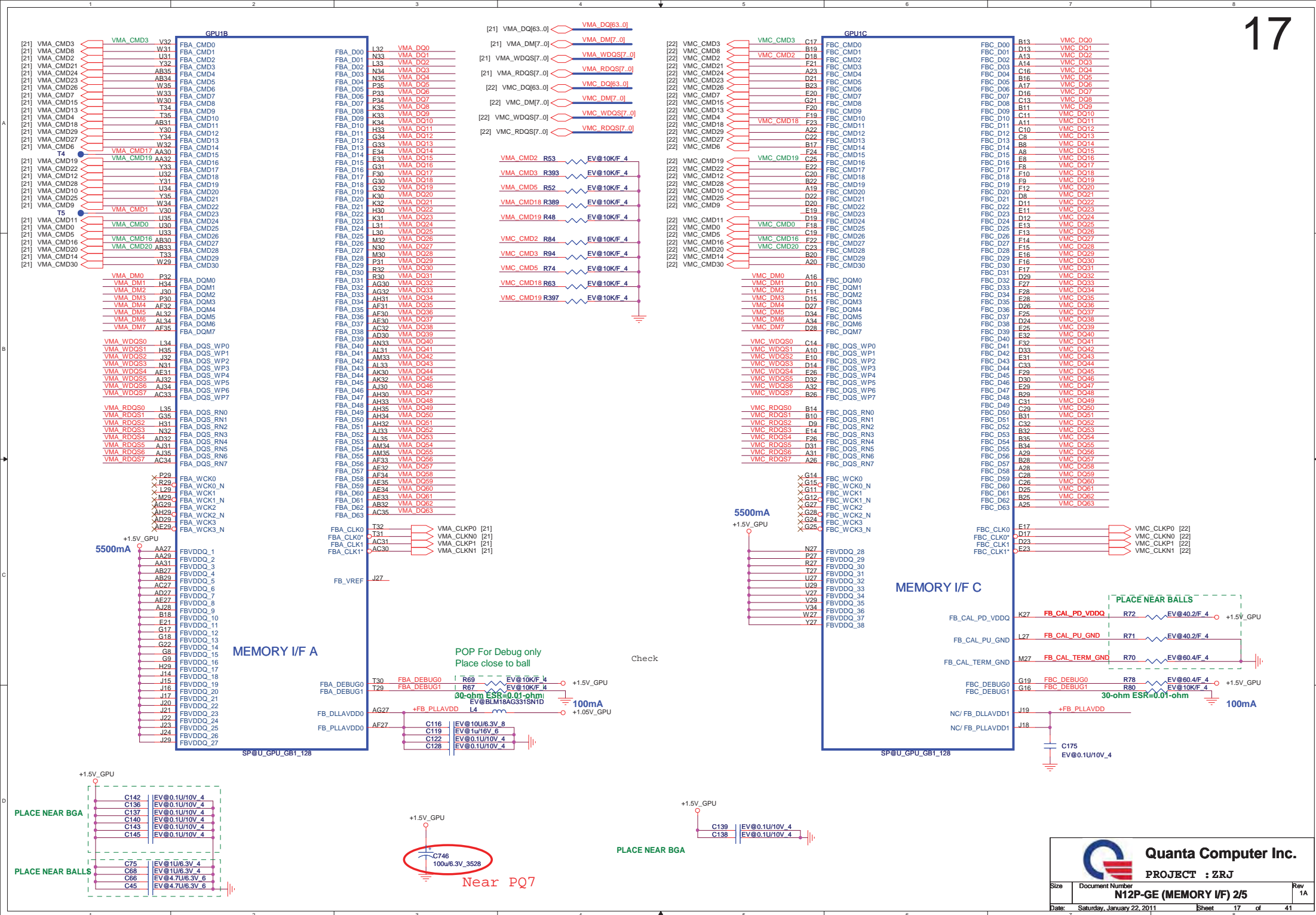


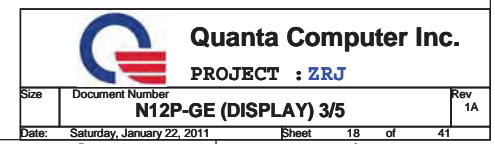
Quanta Computer Inc.

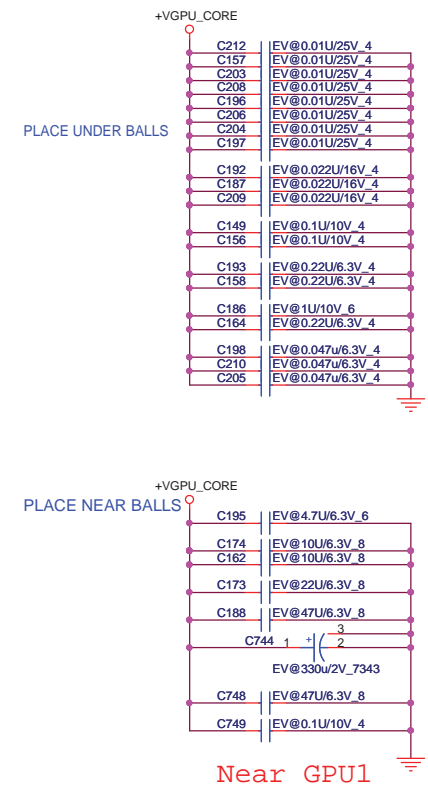
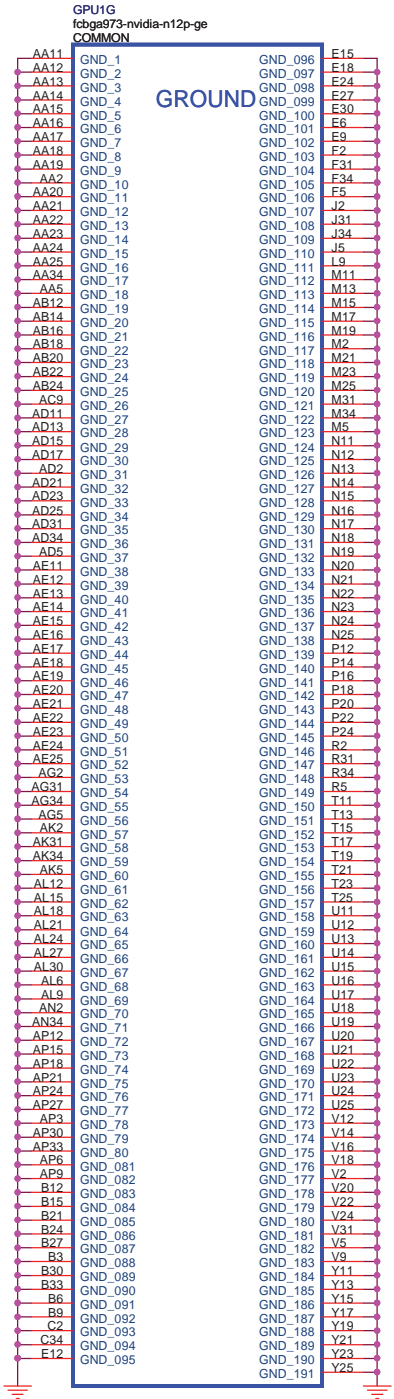
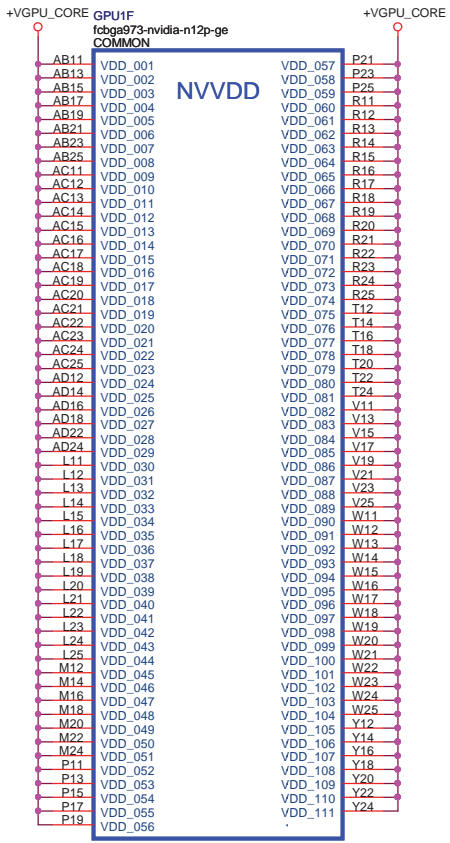
PROJECT : ZRJ

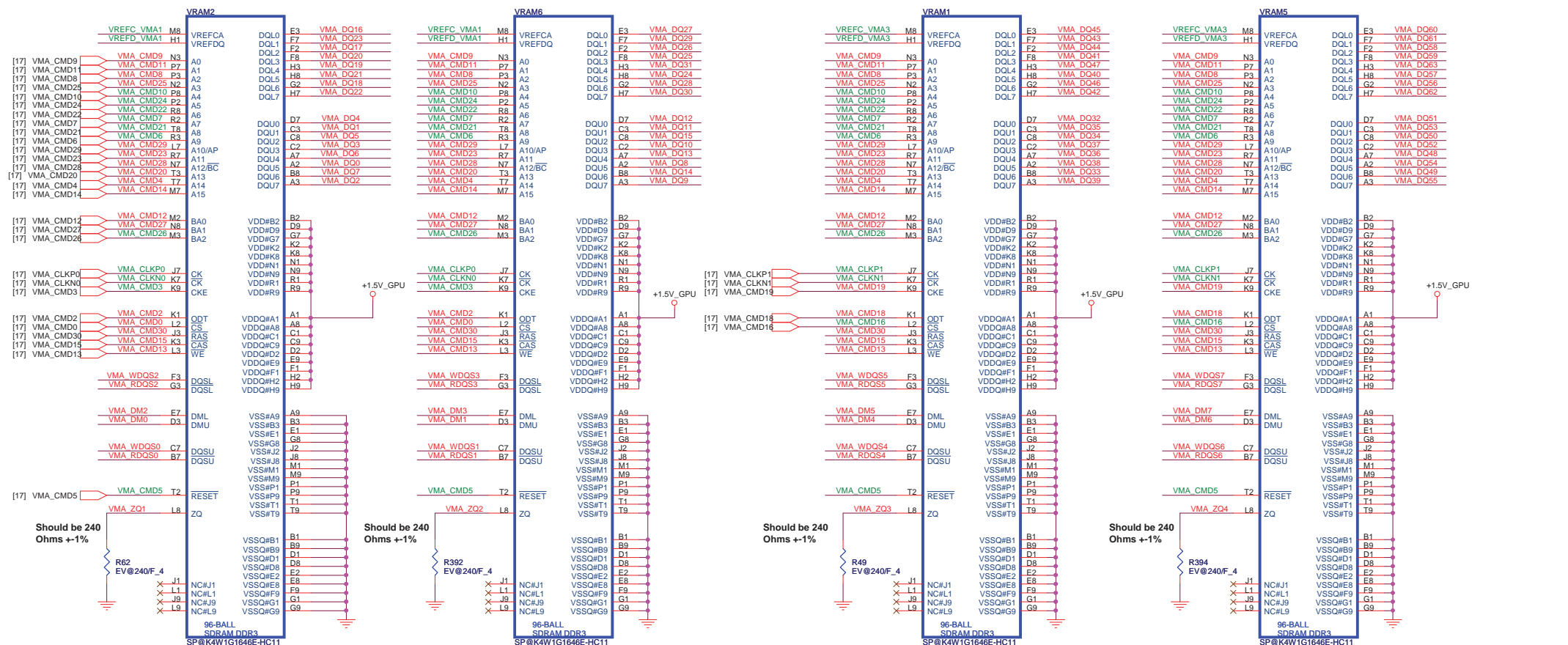
N12P-GE (PCIE I/F) 1/5

Size	Document Number	Rev
Date	Saturday, January 22, 2011	1A
Sheet	16	of 41

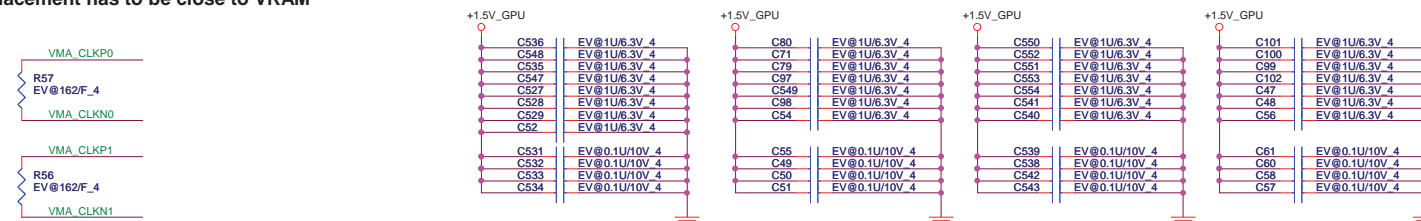


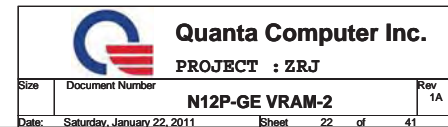
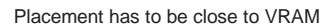


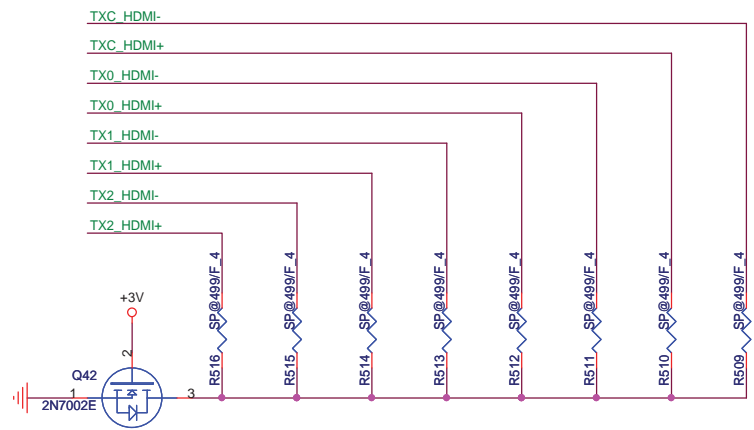




Placement has to be close to VRAM



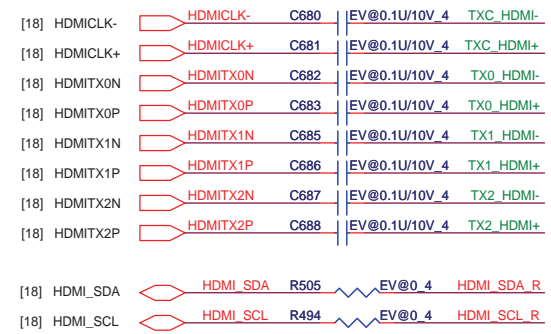




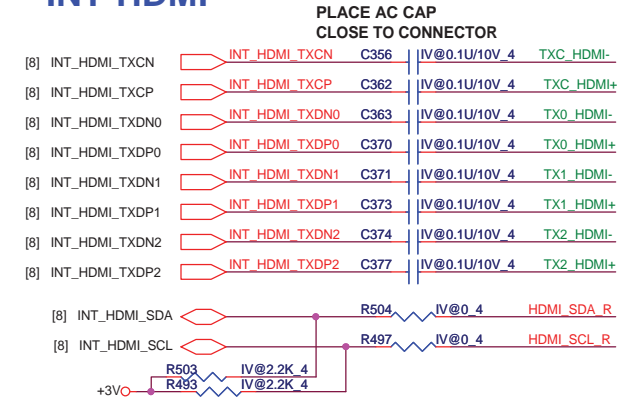
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

	EV@	IV@
SP@	500 ohm	680 ohm

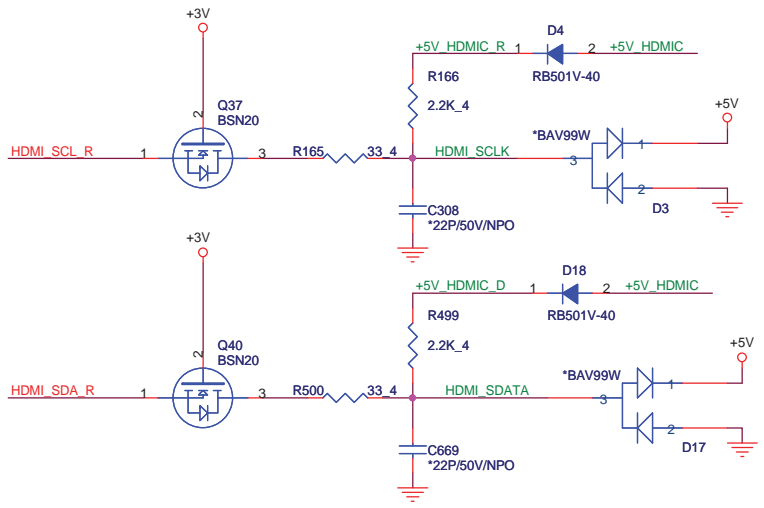
EXT-HDMI



INT-HDMI

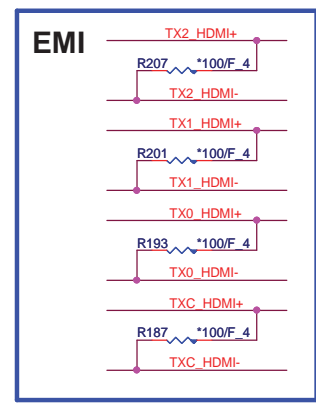


PLACE AC CAP CLOSE TO CONNECTOR

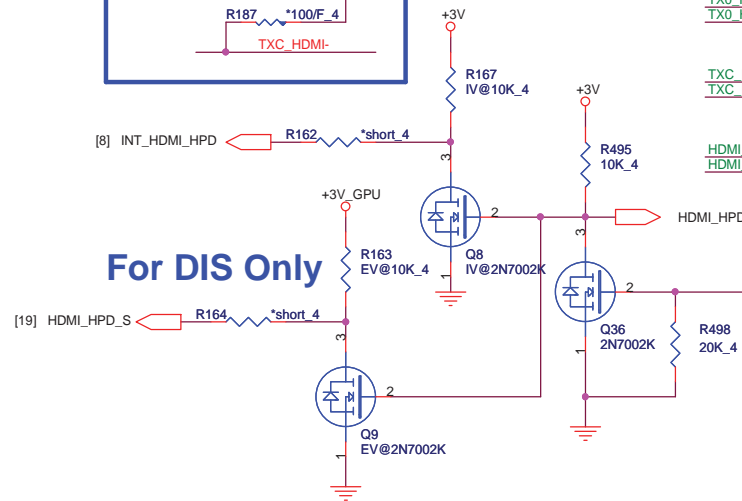


For UMA / Optimus HDMI function

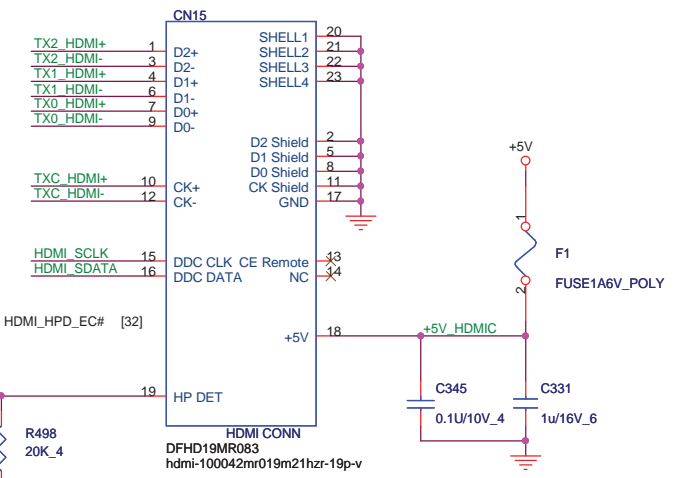
EMI



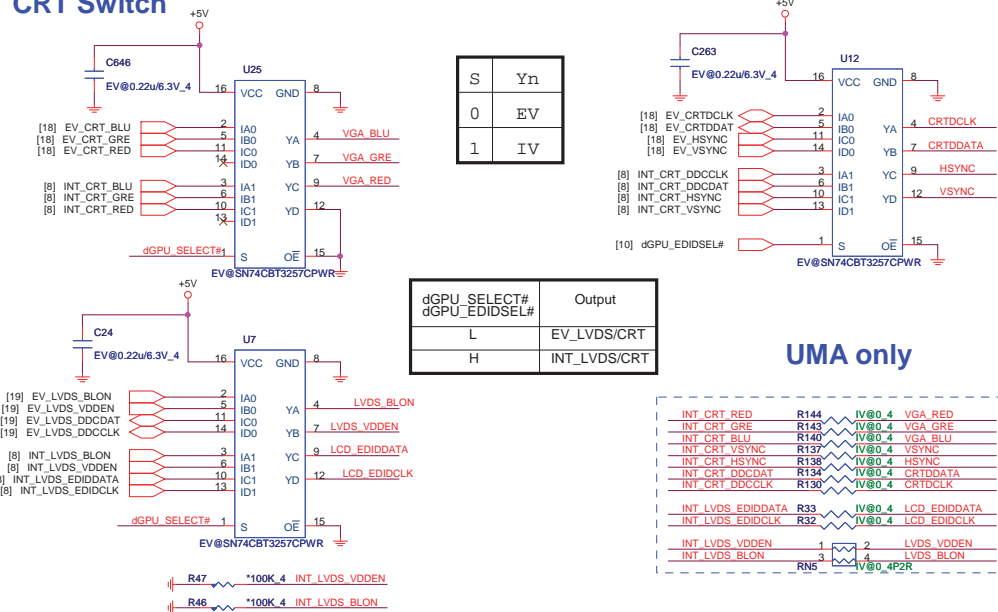
For DIS Only



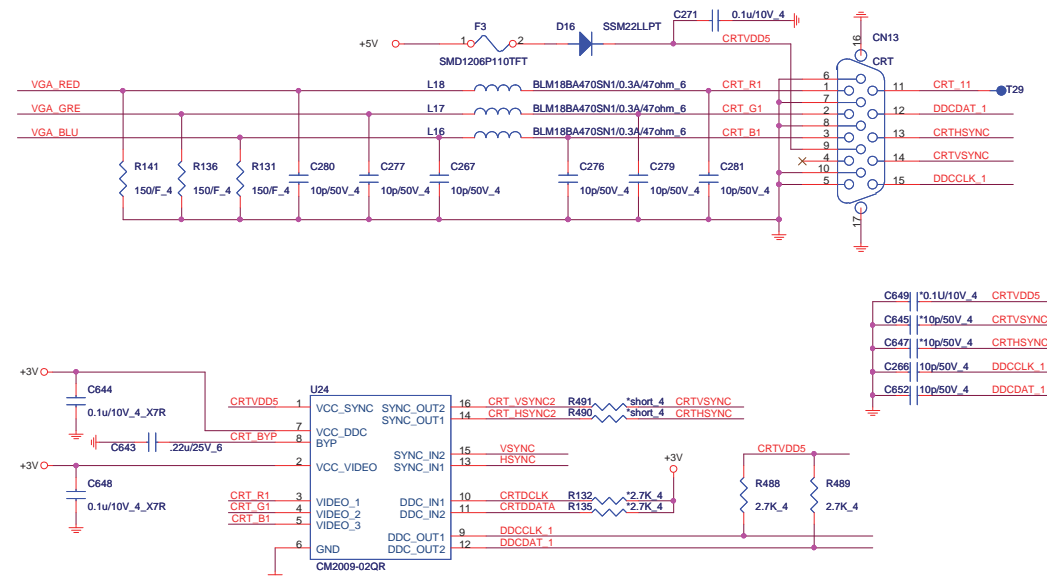
HDMI CONN



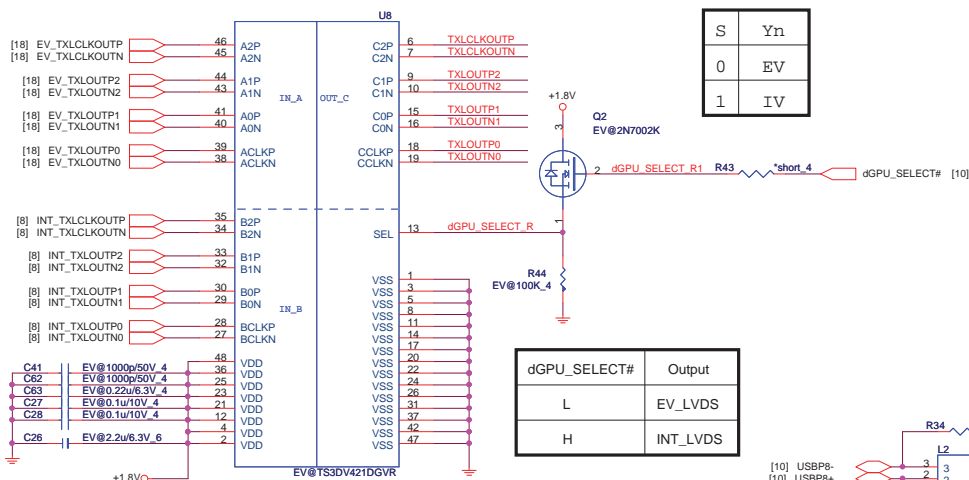
CRT Switch



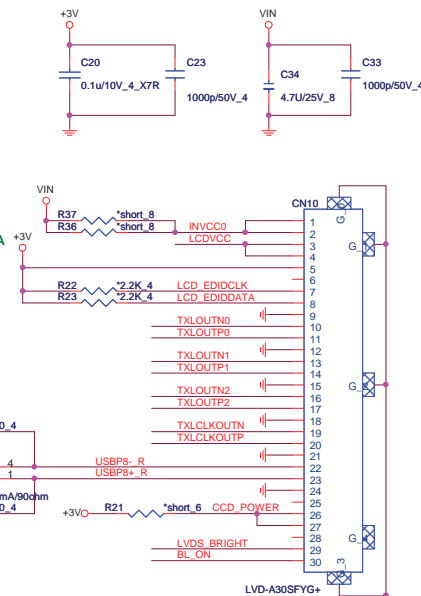
CRT



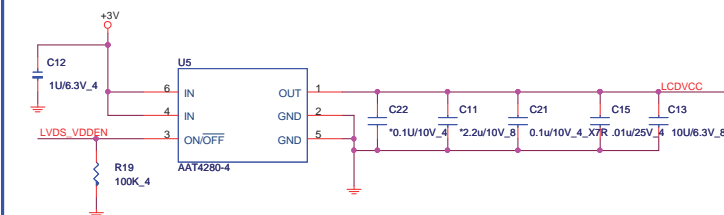
LVDS Switch



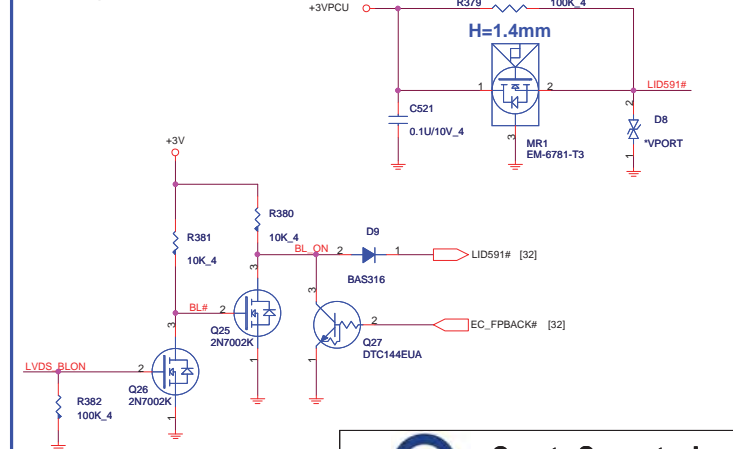
LVDS



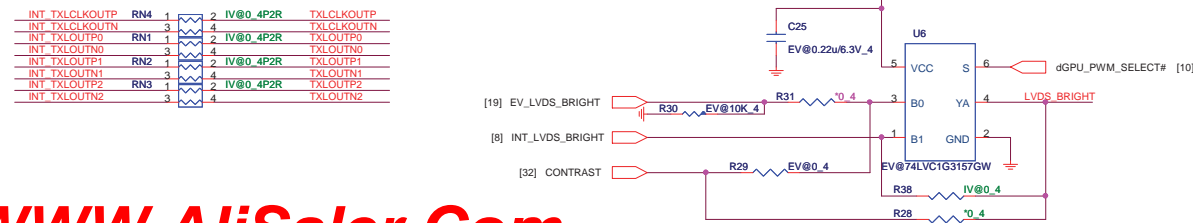
LCD Power



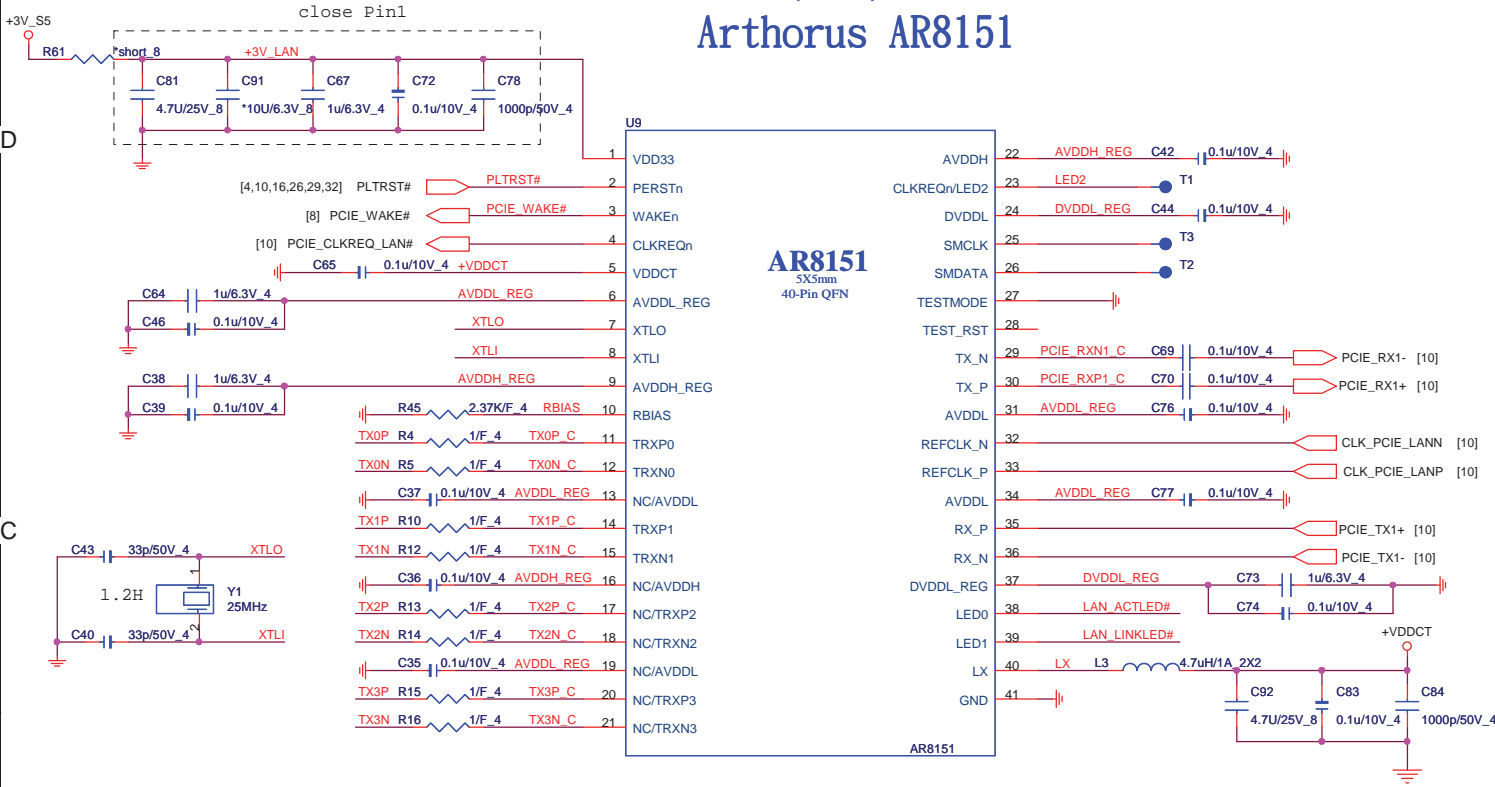
Backlight Control



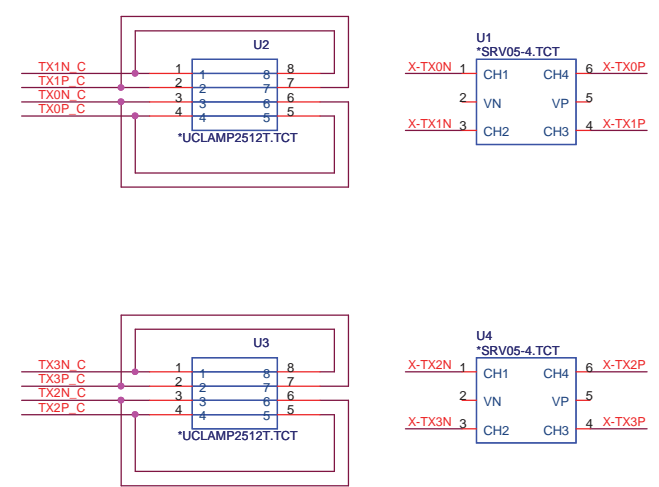
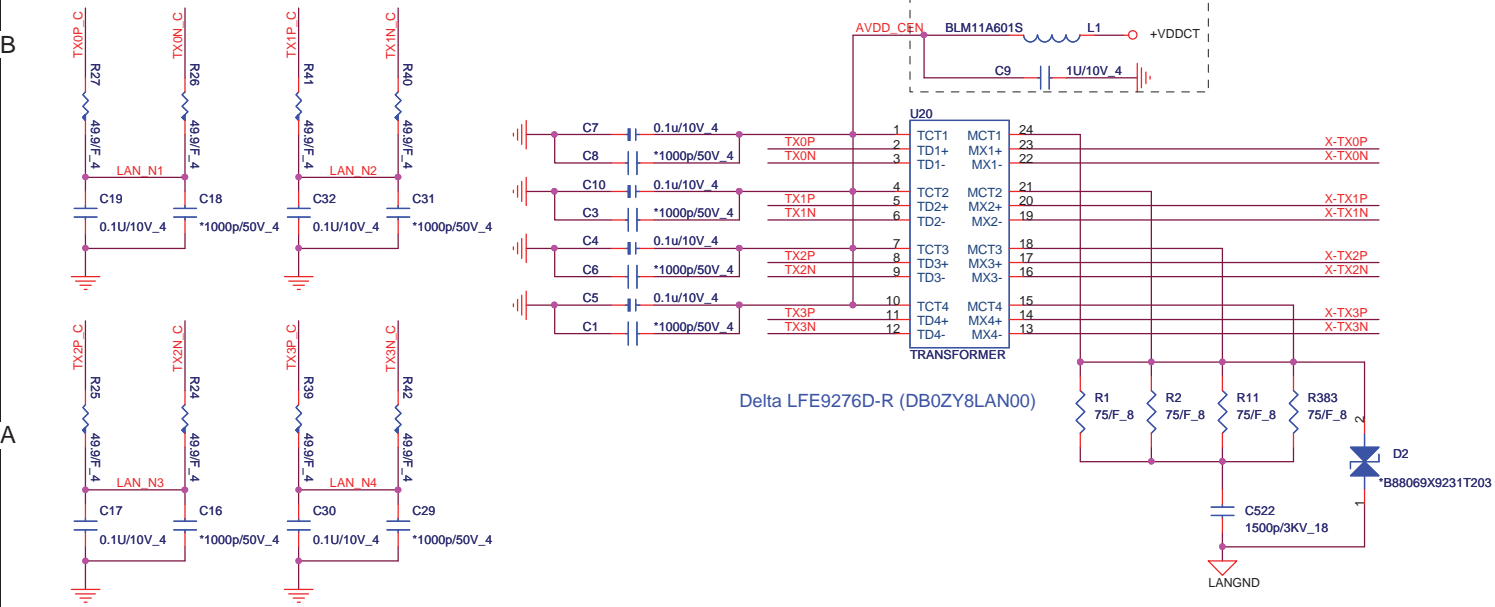
UMA only



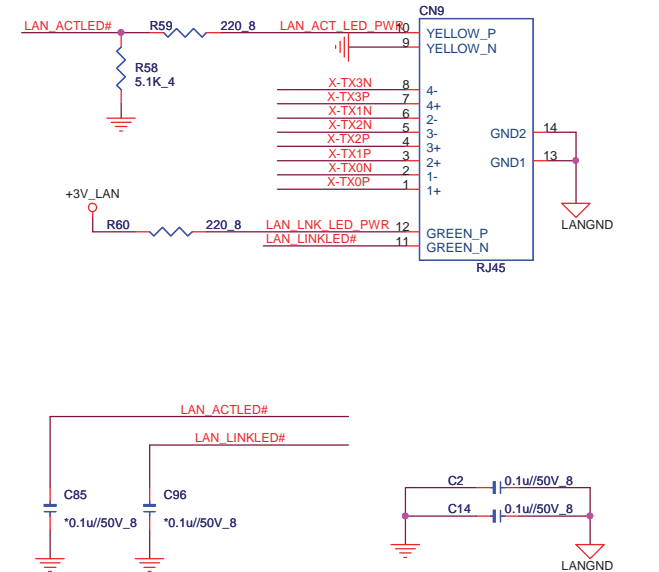
LAN (LAN) Arthorus AR8151



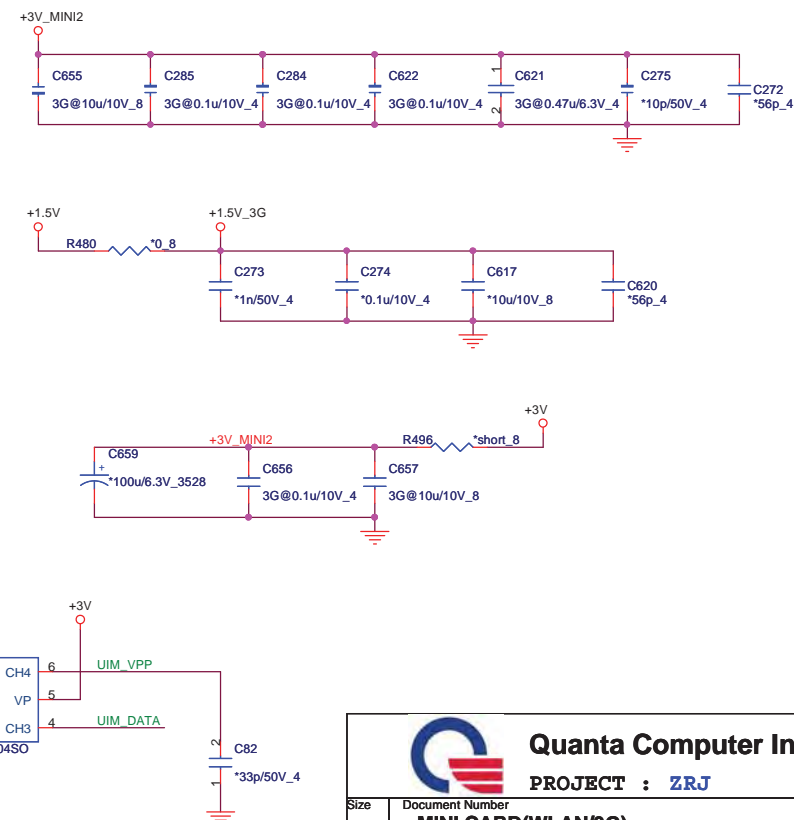
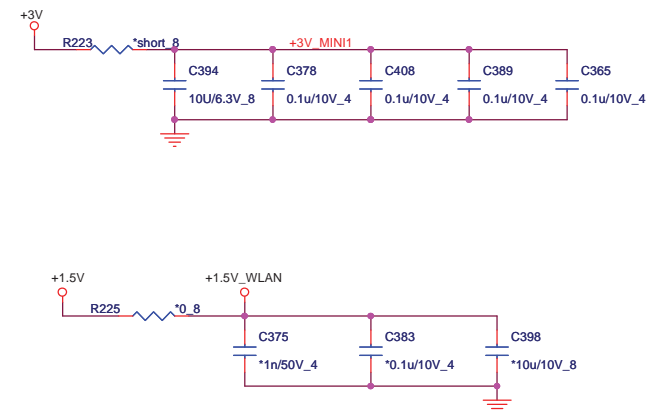
TRANSFORMER(LAN)



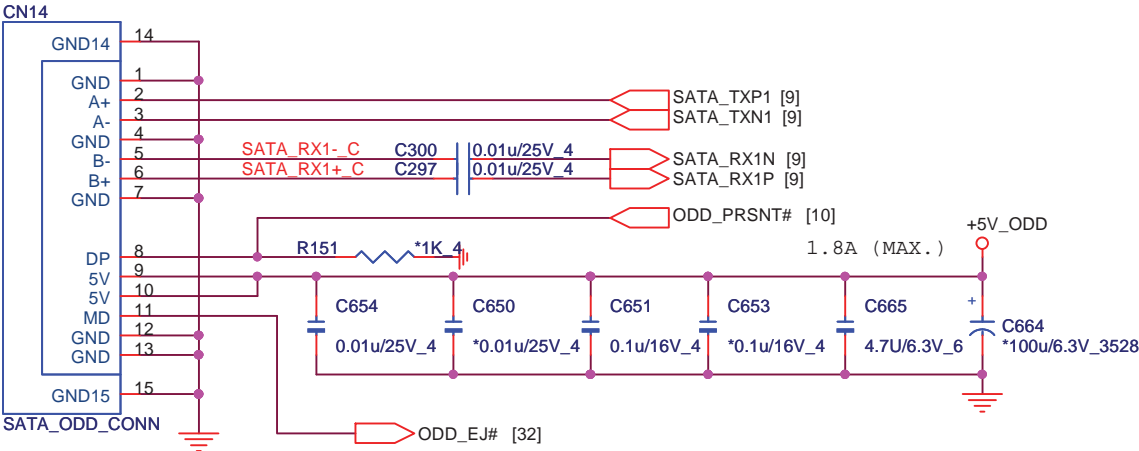
RJ45(LAN)



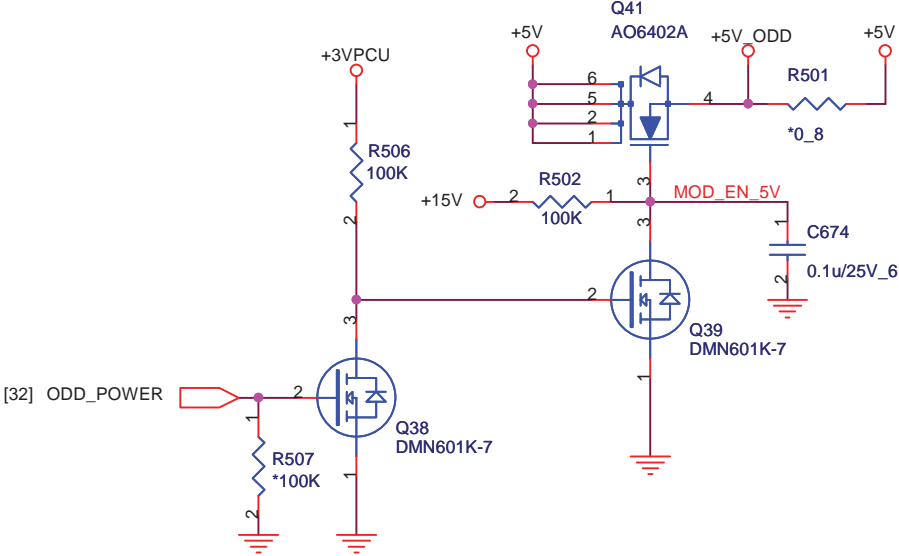
26



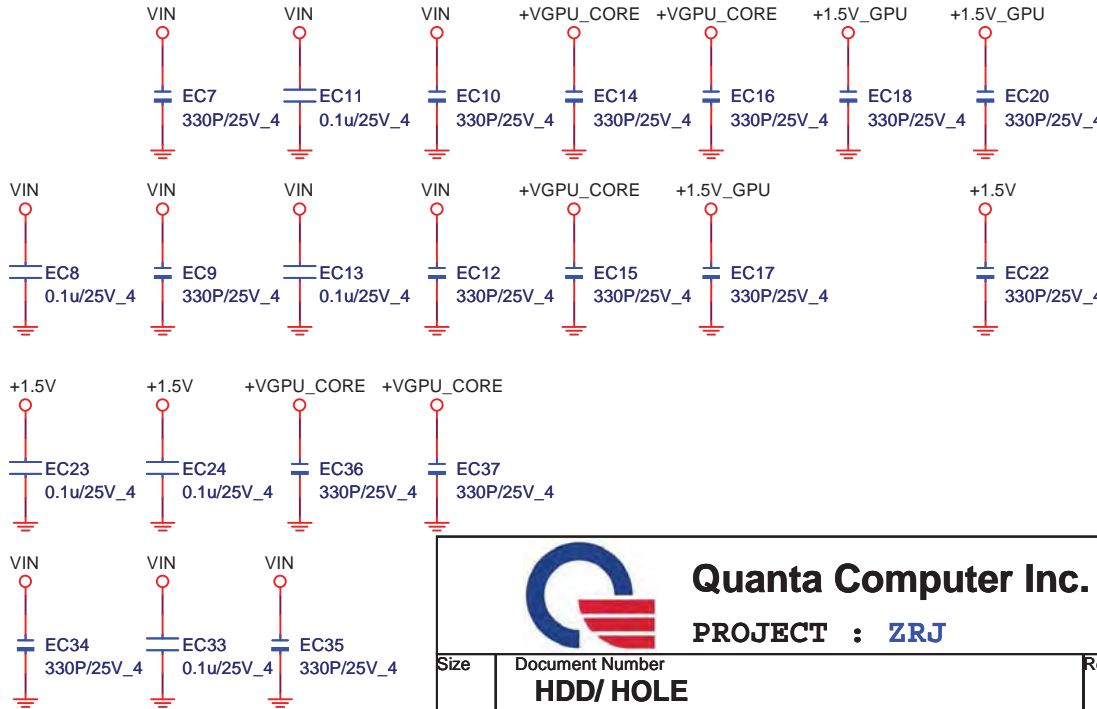
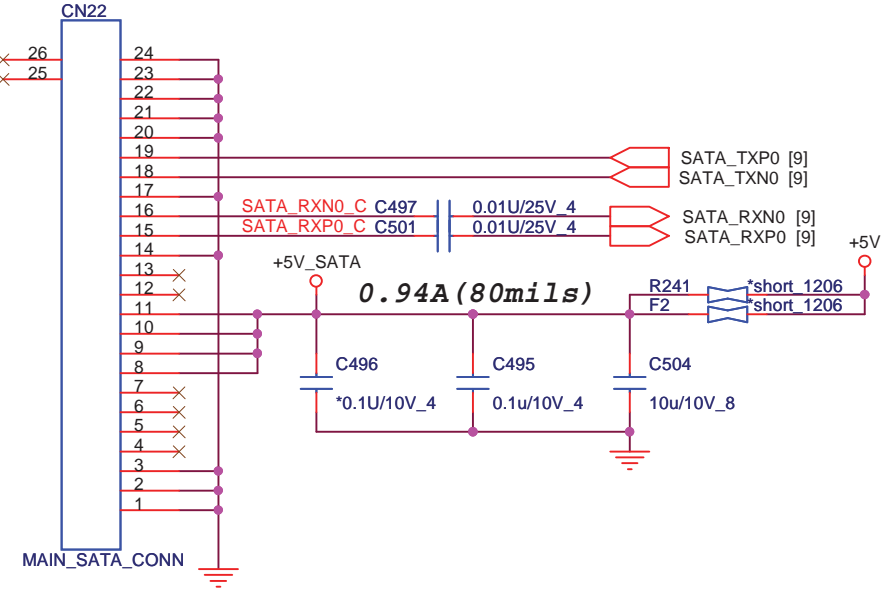
ODD (SATA)




ODD Power (SATA)



2.5" SATA HDD



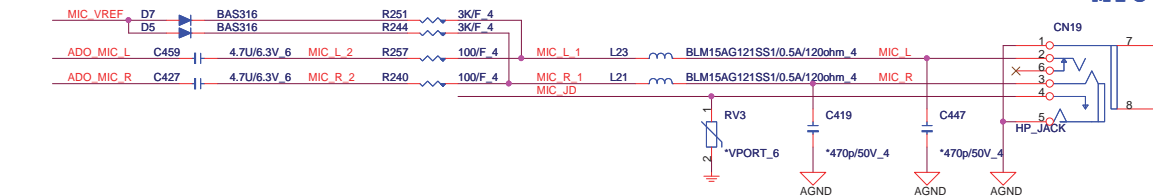


Quanta Computer Inc.

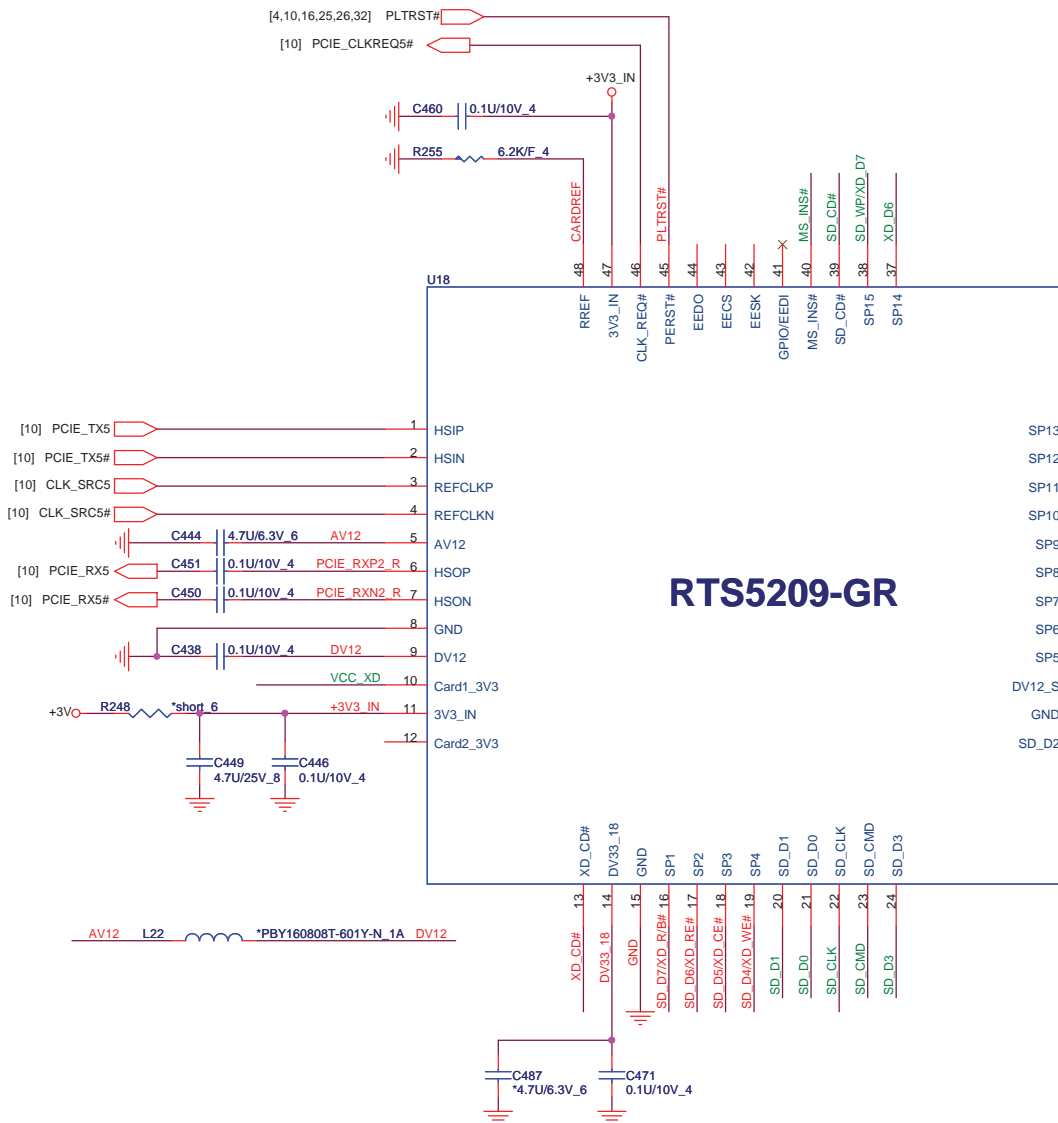
PROJECT : ZRJ

Size	Document Number	Rev
	HDD/ HOLE	1A
Date:	Saturday, January 22, 2011	Sheet 27 of 41

WWW.AliSaler.Com

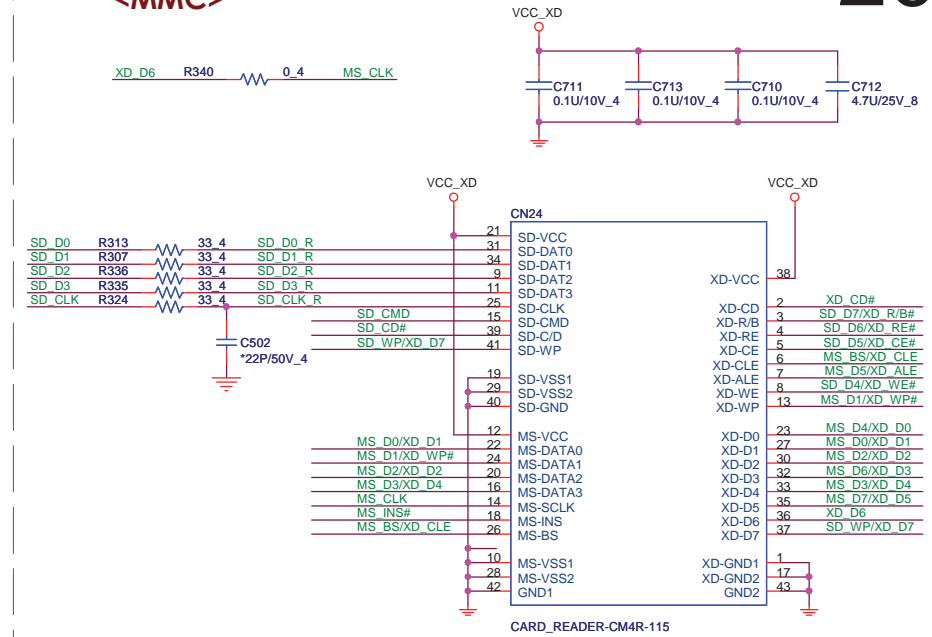


<MMC>



<MMC>

20

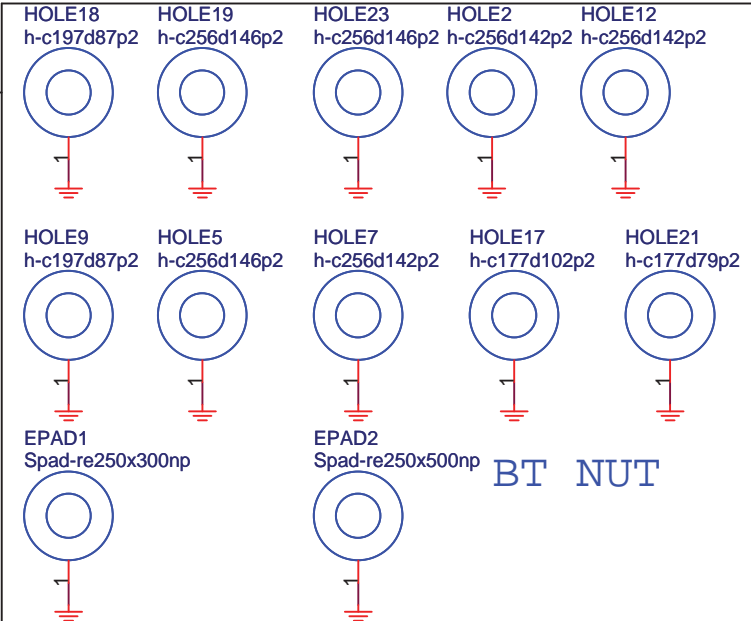
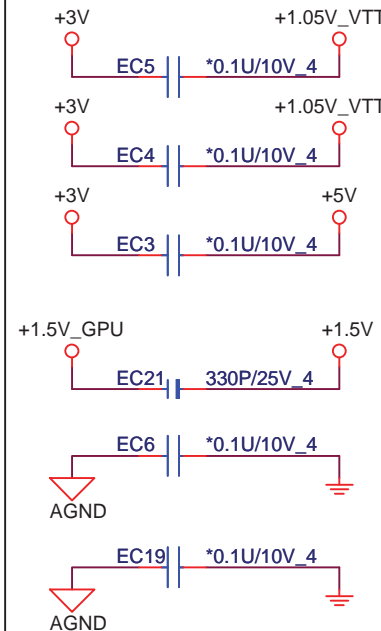
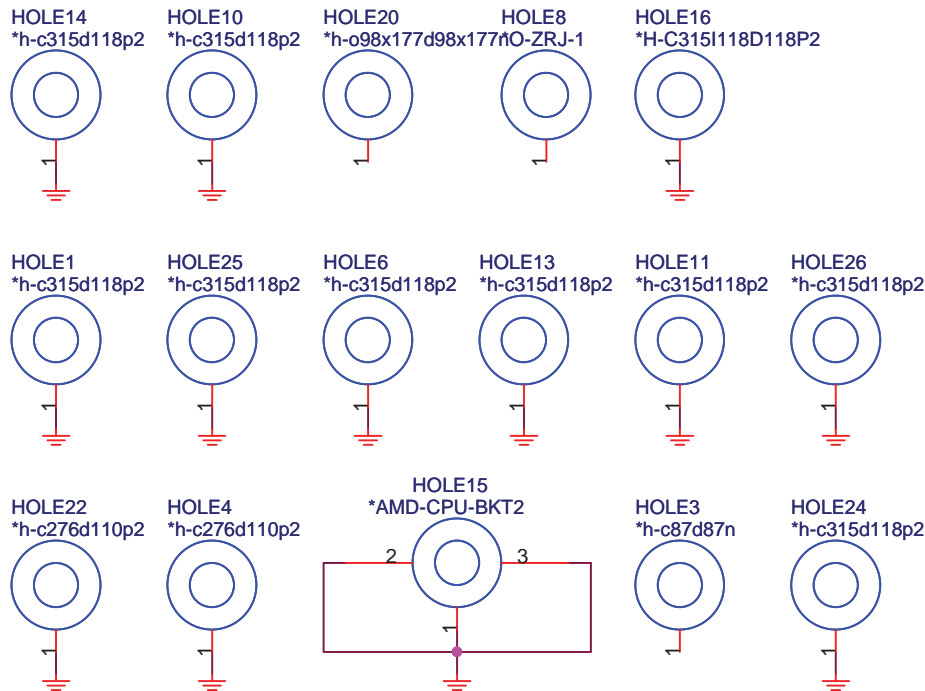
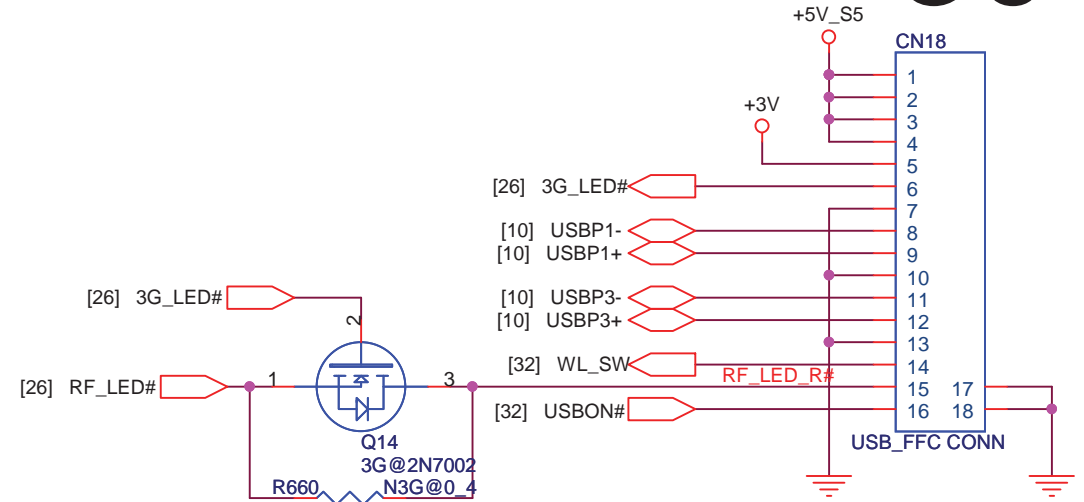
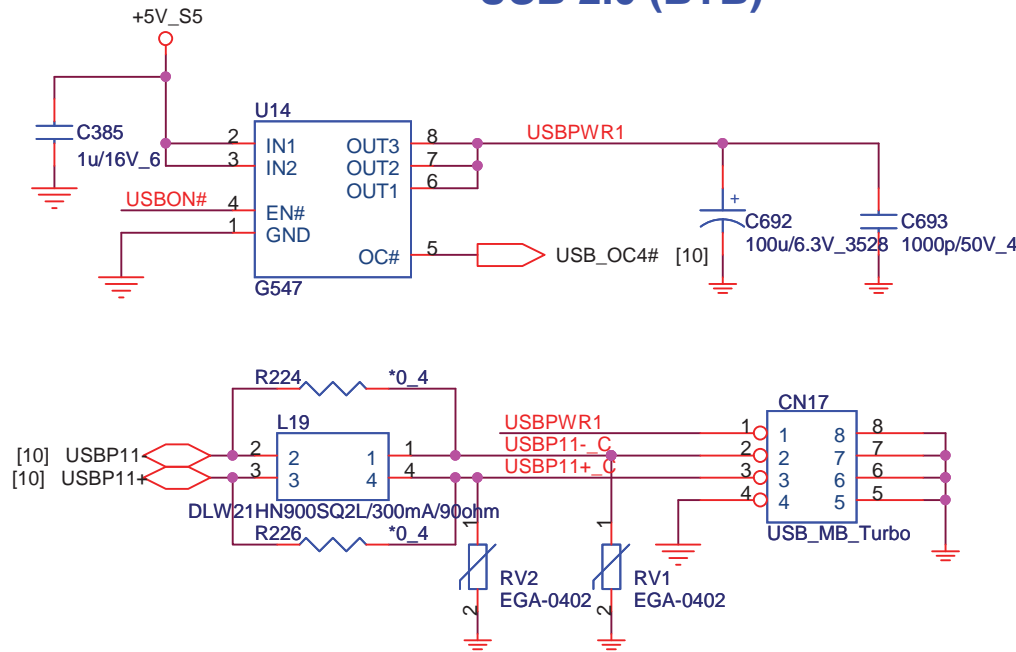



PROJECT : ZRJ

Size	Document Number	Rev
	RTS5209 (Card Reader)	3G
Date:	Saturday, January 22, 2011	Sheet 29 of 41

USB 2.0 (BTB)

30



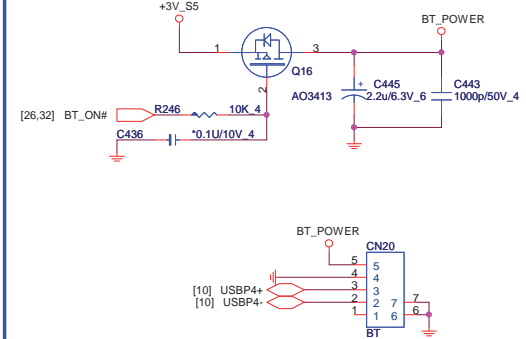


Quanta Computer Inc.

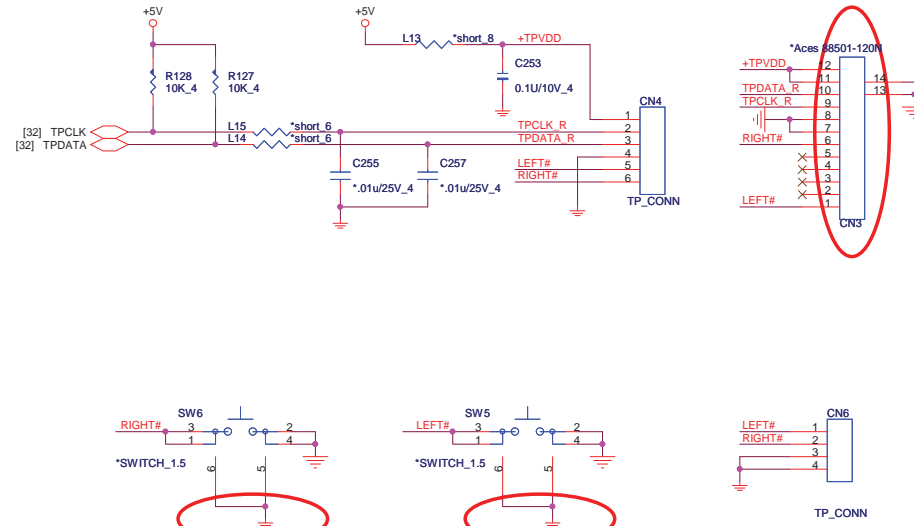
PROJECT : ZRJ

Size	Document Number	Rev
	USB2.0 Board (Dual Way)	1A
Date:	Monday, January 24, 2011	Sheet 30 of 41

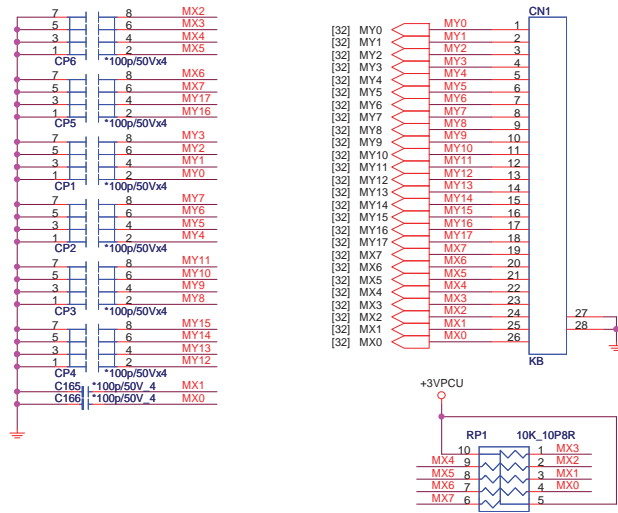
Bluetooth (BTM)



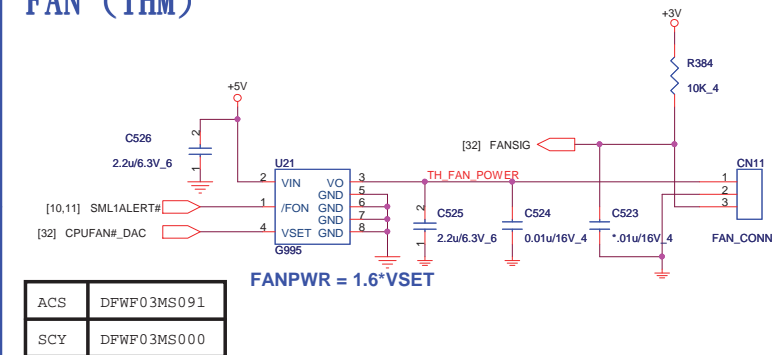
TouchPad (TPD)



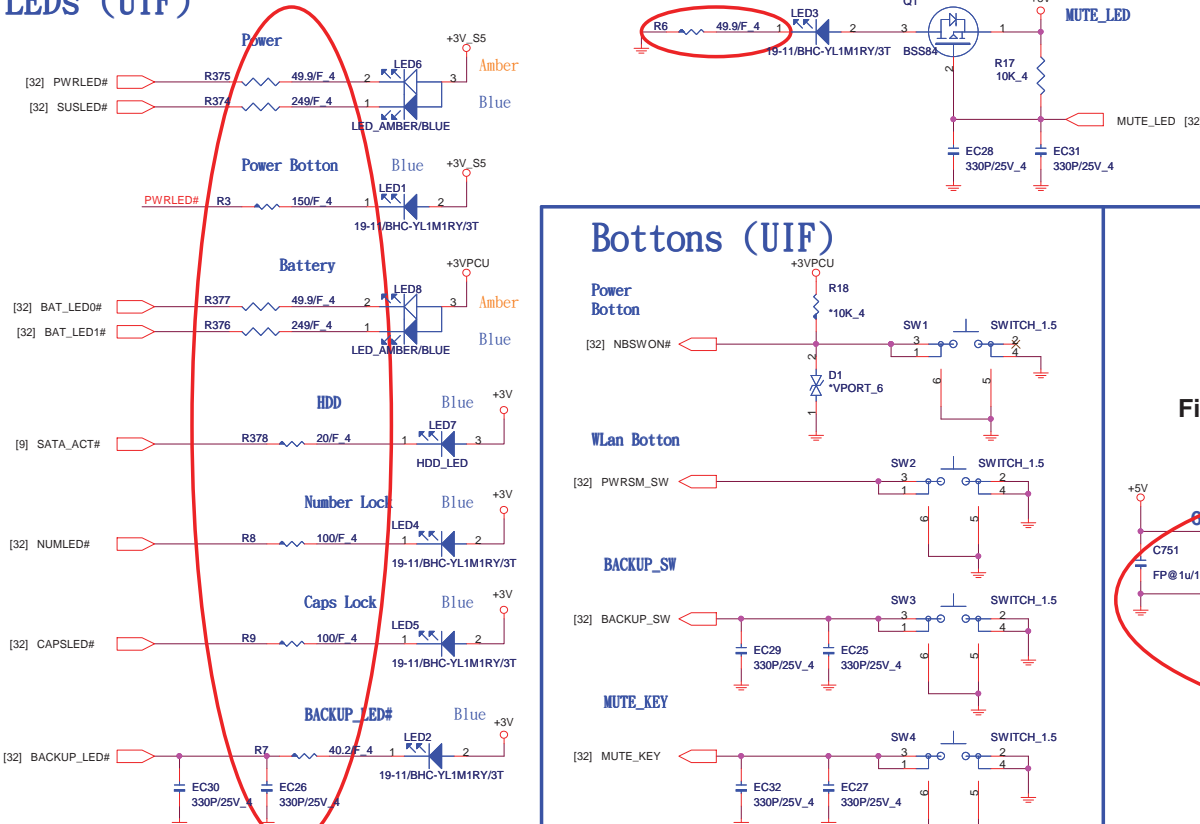
Keyboard (KBC)



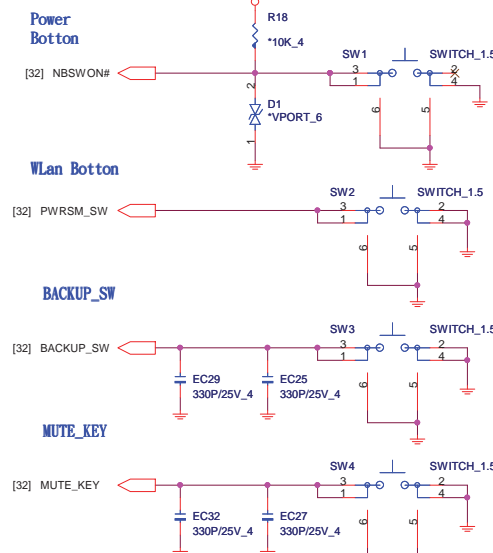
FAN (THM)



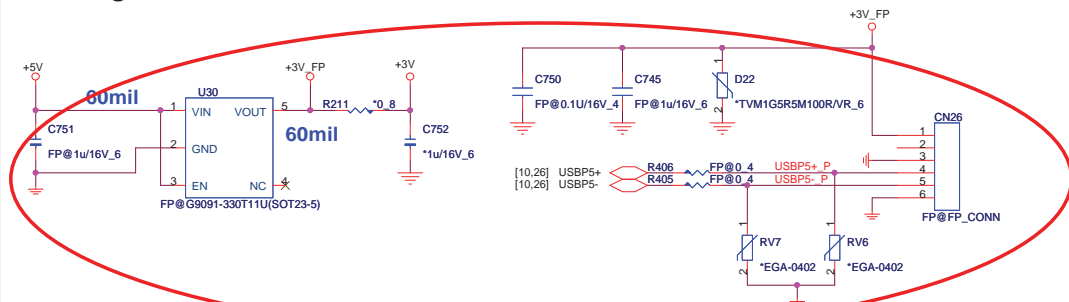
LEDs (UIF)



Buttons (UIF)

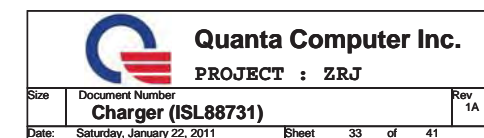


Finger-Printer CONN.

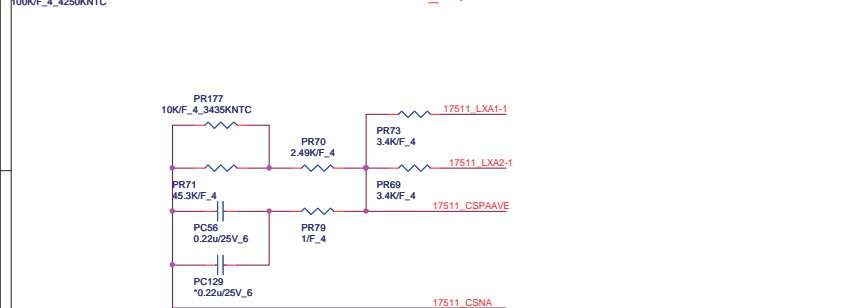


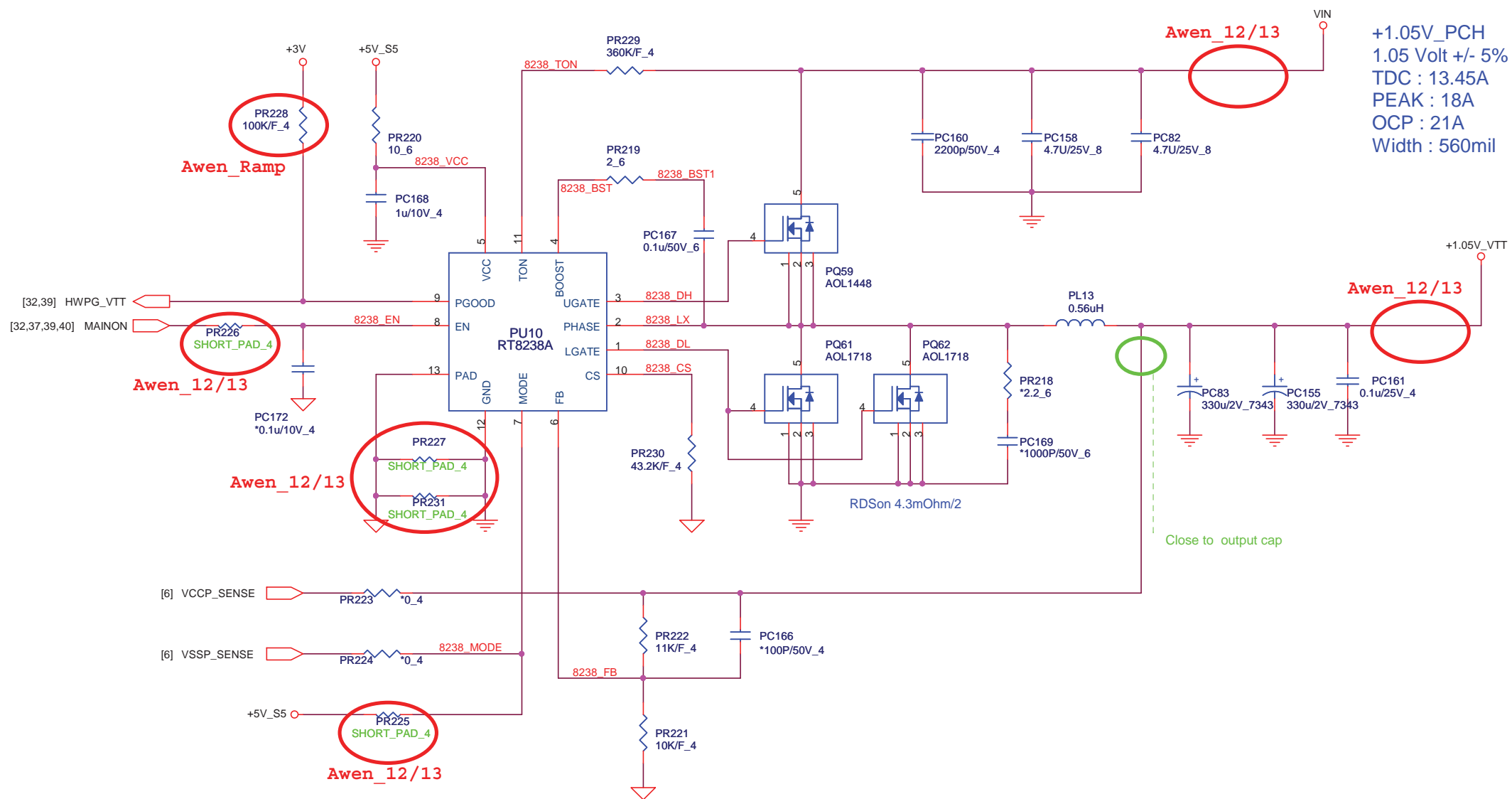
Quanta Computer Inc.

PROJECT : ZRJ



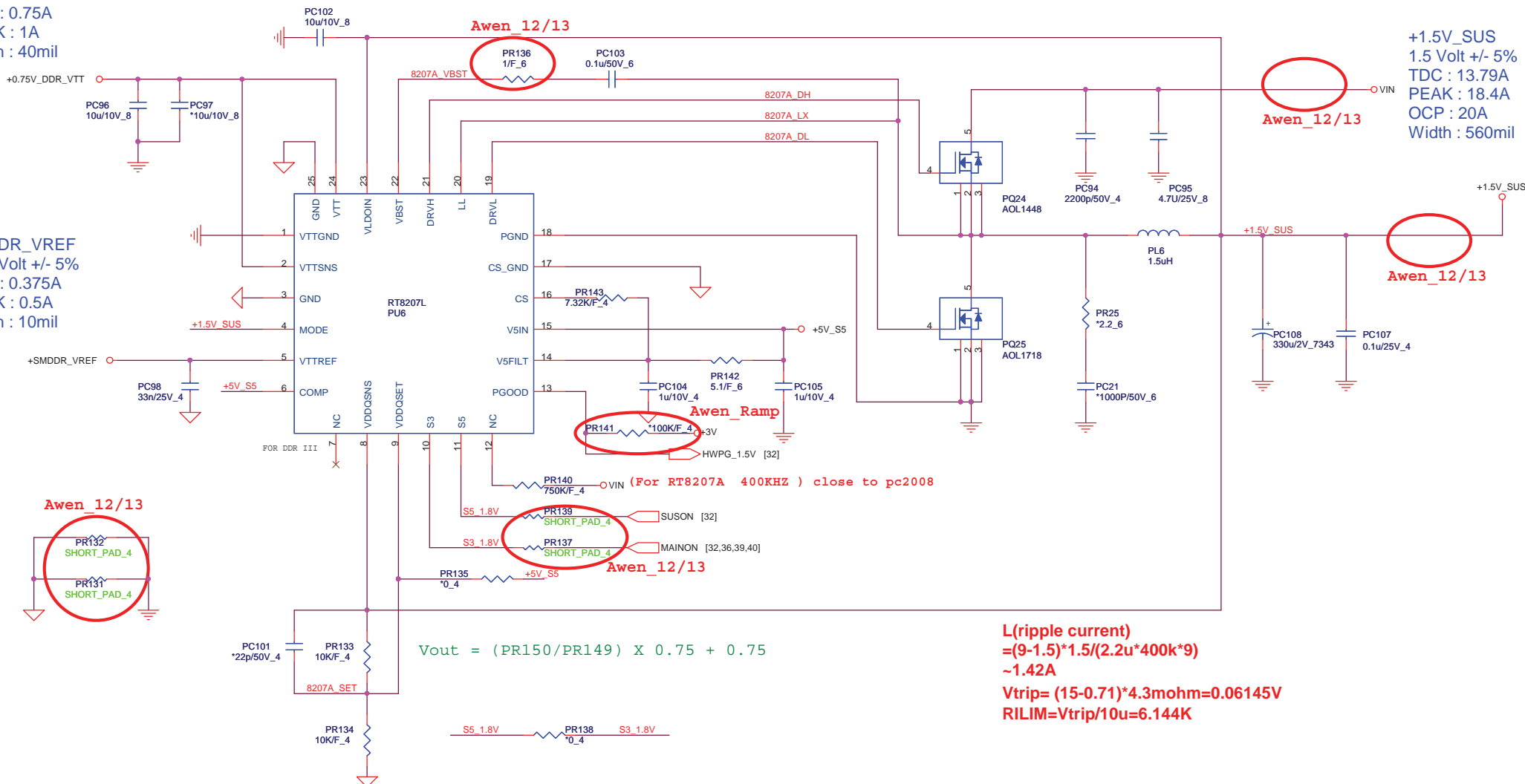




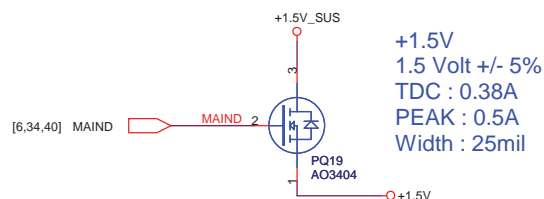


+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.375A
PEAK : 0.5A
Width : 10mil



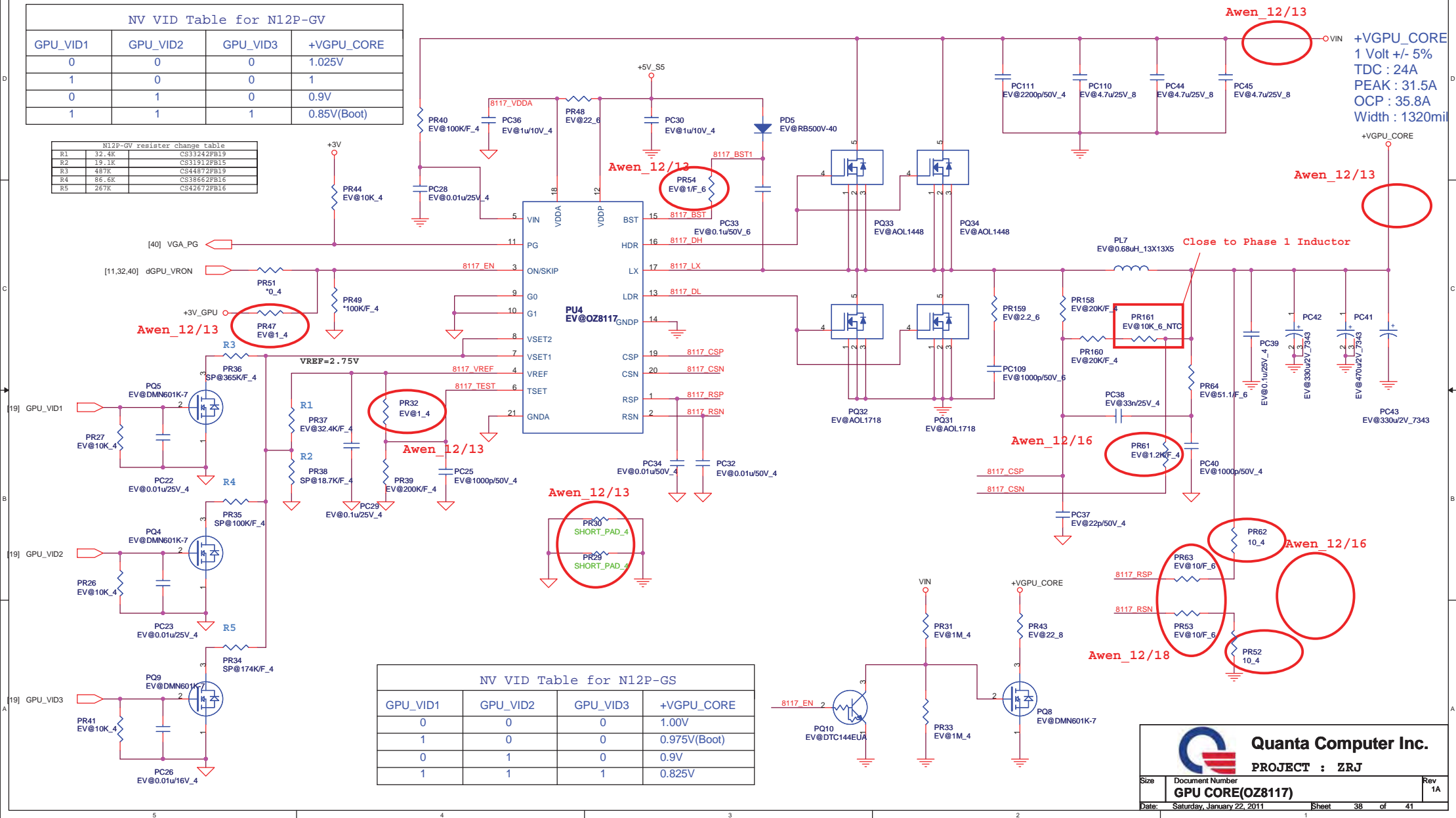
L(ripple current)
 $= (9 - 1.5) \cdot 1.5 / (2.2 \mu \cdot 400 \text{K} \cdot 9)$
 $\sim 1.42 \text{A}$
Vtrip = $(15 - 0.71) \cdot 4.3 \text{mohm} = 0.06145 \text{V}$
RILIM = $\text{Vtrip} / 10 \mu = 6.144 \text{K}$



	S3	S5	+1.5V_SUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (main on off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

NV VID Table for N12P-GV			
GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.025V
1	0	0	1
0	1	0	0.9V
1	1	1	0.85V(Boot)

N12P-GV resistor change table		
R1	32.4K	CS33242F819
R2	19.1K	CS31912F815
R3	487K	CS44872F819
R4	86.6K	CS38662F816
R5	267K	CS42672F816

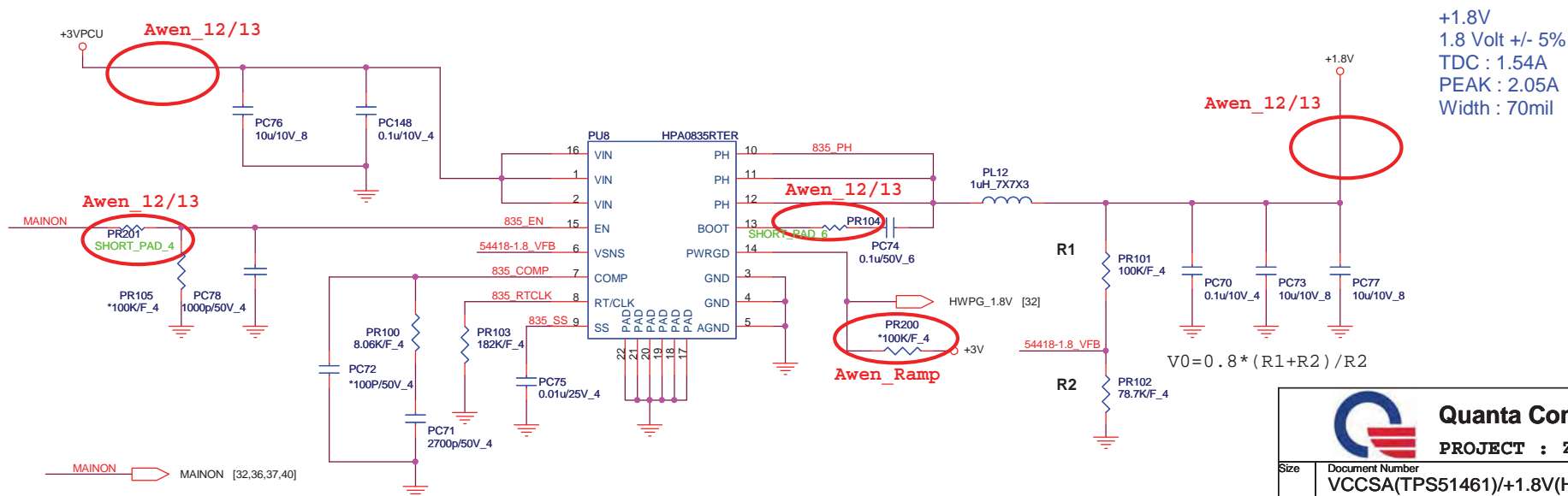
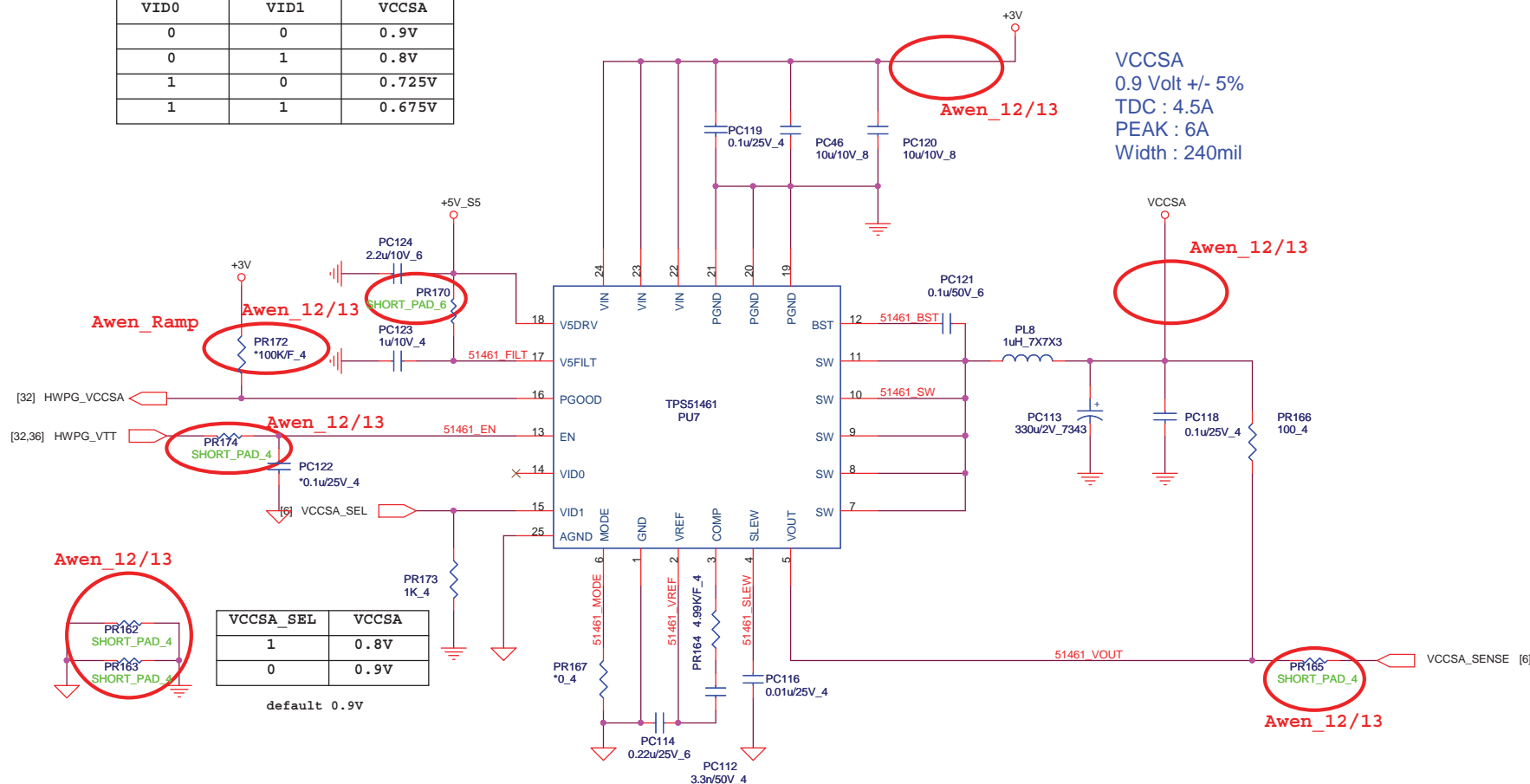


Quanta Computer Inc.

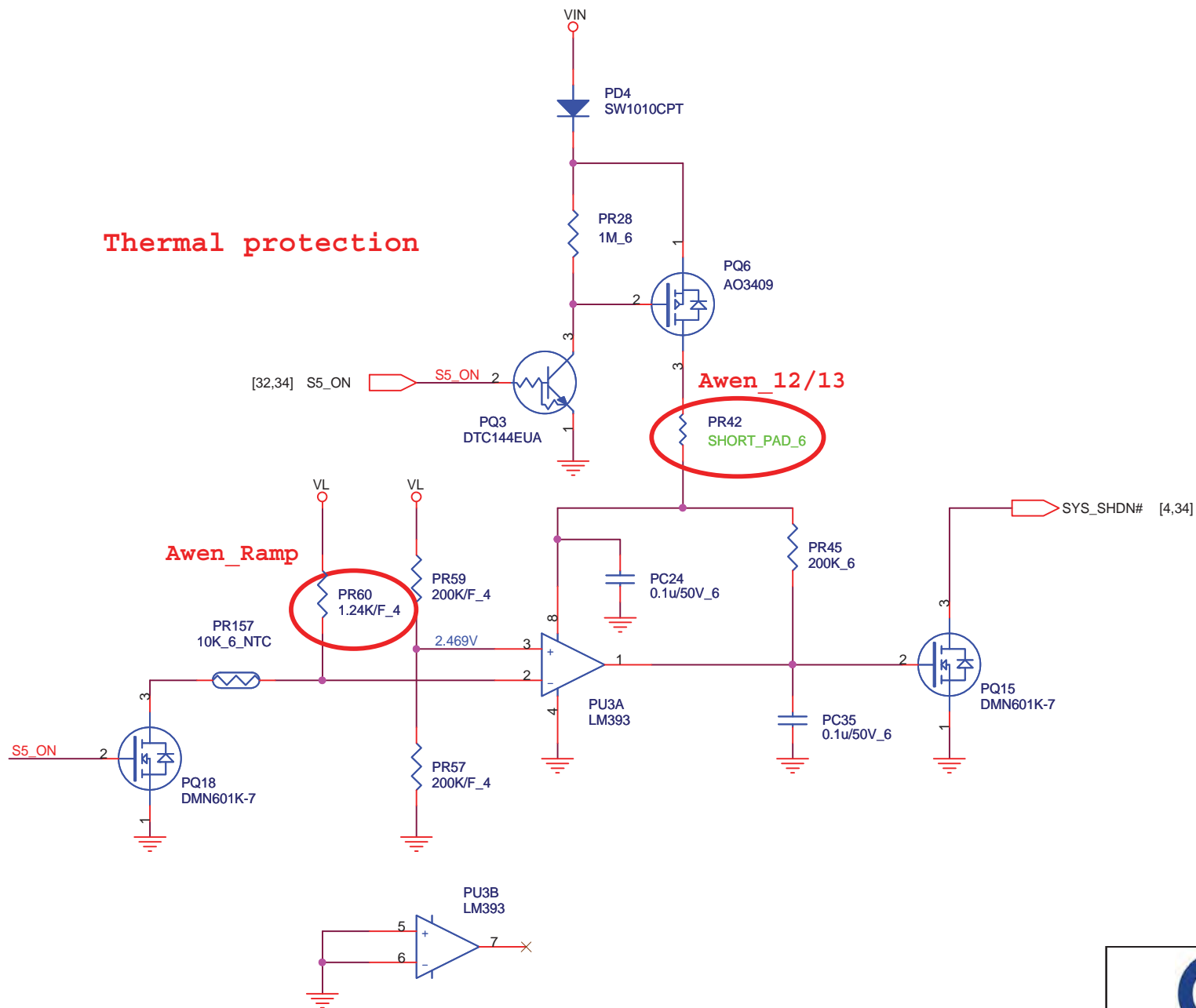
PROJECT : ZRJ

Size	Document Number	Rev
	GPU CORE(OZ8117)	1A
Date:	Saturday, January 22, 2011	Sheet 38 of 41

VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



Thermal protection



Quanta Computer Inc.

PROJECT : ZRJ

Thermal protect

Size	Document Number	Rev 1A
Date: Saturday, January 22, 2011	Sheet 41 of 41	

[illegible]